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PARALLEL INVERTER AND CONVERTER OPERATION AND IMPROVEMENTS IN TRANSFORMERS

(NASA CONTRACT ~~NO.~~ NAS 3-2792)

First Quarterly Report, ~~For The Period~~ June 28, 1963 ~~To~~ September 27, 1963

PREPARED FOR THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

BY:
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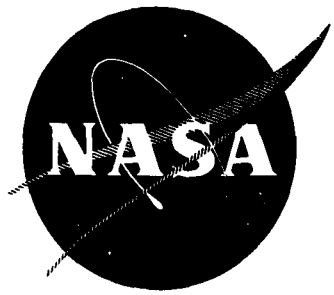

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SUMMARY

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This report describes the analytical and design work completed during the first quarter of the contract period on the design of a static inverter output transformer utilizing field-annealed doubly oriented silicon steel (Cubex steel), and on the development of means for satisfactorily paralleling static inverters and converters.

The output transformer design was completed and is described in this report. Cubex steel has a lower core loss for high flux densities (12-20kg) than do non-oriented silicon steel materials. The use of Cubex core materials should increase the efficiency of the inverter/converter used in the paralleling task. The power-to-weight ratio could have been increased by keeping efficiency constant.

The necessary conditions for satisfactory paralleling of static inverters and converters were considered mathematically to determine circuit design criteria. Methods of paralleling were chosen and circuits were designed for applying these methods to an existing high-performance static inverter/converter design.

The development of a paralleling method is expected to increase the reliability and output power capabilities of inverter/converter systems.

Author

I. INTRODUCTION

The purposes of this program are to improve inverter transformer weight and efficiency characteristics through the application of field-annealed, doubly oriented silicon steel magnetic core material (Cubex steel), and to improve inverter/converter reliability and power capability by developing means for parallel operation of static inverters (DC-AC) and converters (DC-DC). These two tasks will be discussed separately.

Task I - Cubex Transformers

Cubex steel is a magnetic material being developed by Westinghouse Electric Corporation. Magnetic materials normally used for "EI" type transformer laminations are not grain oriented and have comparatively high excitation losses. Cubex steel is doubly oriented and has two "easy directions" of magnetization perpendicular to each other within the plane of the laminations. This double orientation makes Cubex steel very suitable for "EI" type laminations. It has much lower excitation loss than the non-oriented steel normally used for these type laminations.

One output transformer will be made from Cubex steel for evaluation in the inverter/converter models which will be built for the paralleling task. This "quadratic" transformer uses special "EI" type laminations and is expected to utilize the features of Cubex steel to result in a very efficient, lightweight transformer for inverter applications.

Task II - Parallel Inverters/Converters

Static inverters/converters are often used in satellites and similar long-life, low-maintenance missions. The problem of reliable operation throughout the life of the mission is very critical. Each time a different mission is defined, a different inverter of the desired rating is required. The size and complexity of an inverter depends on the value of the input voltage and on the limitations of the semiconductors used. Each new inverter must be tested and modified until the desired degree of reliability is obtained. The desired reliability could be obtained through redundancy; i.e., by having several system-rated inverters on standby. Thus, if the main inverter fails, one of the standby inverters will take over, etc. The desired reliability can be obtained in this manner, but the system weight will be high.

A more desirable solution to the weight-reliability problem would be the use of several smaller highly developed inverters in parallel. The system rating and the desired reliability could be obtained in this manner. A new system would be built by the addition or deletion of some of the inverters.

The requirements of this study are:

1. Each inverter must be capable of operating independently.
2. Each inverter must be capable of operating in parallel with any number of similar inverters.
3. There must be provisions for automatic voltage regulation and load sharing.

The proposed method of operating static inverters in parallel is described in this report and consists basically of the following:

1. Interconnect all inverter control circuits so that the phase-A no-load output voltage of each inverter is in phase with the phase-A no-load output voltage of all other inverters before paralleling. The phase sequence of all inverters must be the same before paralleling.

2. After paralleling two (or more) inverters, the magnitude of the "internal" voltage of each inverter is controlled so that load current is divided equally between (or among) inverters. ("Internal" voltage of an inverter is defined as the imaginary voltage behind the internal impedance of the inverter. The "internal" voltage equals the output terminal voltage only at zero load.) This control is achieved by making the internal voltage regulator sensitive to both terminal voltage and certain components of the differential load current. (Differential load current is the difference between an actual inverter output phase current and the average of all inverter output currents of the same phase.) The component of the differential current to which the internal voltage regulator must be made most sensitive can be calculated after the internal impedance of the inverter has been determined. Procedure for these calculations is given in this report.

Static converter paralleling techniques are less complicated than those of static inverters. The only requirements are that the converters have the same nominal-requlated-terminal voltage and that some means be available to cause the converters to share load current. The load sharing circuits are described in the text of this report.

II. STATEMENT OF WORK

The objectives of this program as defined by NAS3-2792 are two-fold in nature:

1. To investigate the means of decreasing weight and improving efficiency of transformers for static d-c to a-c inverter and d-c to d-c converter circuits.

2. To determine a means whereby inverters and converters can be successfully paralleled to increase system reliability and output power at reduced overall weights.

To accomplish these objectives, the following work tasks have been initiated:

Task I - Transformers

Design and fabricate a test sample transformer utilizing field-annealed, doubly oriented silicon steel magnetic core material. Test and evaluate performance of this sample in an inverter circuit and compare results with those of conventional transformer core materials.

Task II - Parallel Operation

1. Mathematically establish the requirements for satisfactory paralleling of inverter and converter circuits. Determine the optimum method for meeting these paralleling requirements, and design circuits for automatically locking independent frequency references together and automatic voltage regulation and load sharing.

2. Build two static inverter models of an existing design and incorporate the paralleling circuits described above. The static inverter models shall be easily changed to converter operation. Using these models, demonstrate feasibility of paralleling inverters and converters. Assemble data which will sufficiently prove that paralleling has been successfully accomplished.

3. Test and evaluate the systems to completely determine performance characteristics including, but not necessarily limited to, the following:

   (a) Division of real and reactive loads at various power factors.
   (b) Effects of overloads and various fault conditions.

(c) Voltage regulation and frequency stability at 25%, 50%, 75%, 100%, and 125% loads.

(d) Prepare a qualitative description of the factors contributing to increased system reliability at reduced weight resulting from paralleling inverters and evaluate the increases in reliability and system weight reduction which may, thereby, be possible.

III. DESIGN OF STATIC INVERTER OUTPUT TRANSFORMER UTILIZING FIELD-ANNEALED DOUBLY ORIENTED SILICON STEEL

A. Material Characteristics.

Doubly oriented silicon steel, known as "Cubex", has two easy directions of magnetization rather than one as in conventional grain oriented magnetic steels. An easy direction is defined as the direction of magnetization that results in the lowest loss for a given flux density. Most steels have one easy direction, usually in the direction it was rolled. Cubex steel has two easy directions, one perpendicular to the other. Core configurations that require flux to traverse the core in the plane of the laminations take advantage of the two easy directions property. A tape-wound core (toroidal) is an example of a configuration that uses only one direction of magnetization. Preliminary indications are that a technique using a magnetic field while annealing, will result in lower losses for this material when the exciting frequency is 400-cps or above. Comparative test results, using this magnetic material in toroidal cores, was given in a District Paper written by Dr. A. C. Beiler*, and presented at the District 11 and 14 IEEE meeting on May 8, 1963. This paper, "Cubex Magnetic Cores for Aerospace Electrical Equipment", will be included as an Appendix in the second quarterly report.

It is expected that "Cubex" material characteristics can be used in static inverters and converters as a means of increasing efficiency and/or reducing weight. The lower loss characteristic at higher frequencies should be particularly well suited to the "square wave" voltages which are commonly found in inverter/converter circuits and which are rich in high harmonic frequencies. The two easy directions of magnitization should make this material suitable for a variety of E-I type lamination configurations. For this type of transformer construction, non-oriented materials are normally used which require higher exciting currents and have higher losses or must be operated at lower flux densities.

For this program, two identical output transformers will be built using 11-mil magnetic material (Hipersil, 3% silicon - 97% iron). These transformers will be connected into the inverter models during the paralleling test program. Another transformer of the same design will be made using 6-mil "Cubex" magnetic core material. This transformer will be evaluated in one of the inverter models to determine what improvement in efficiency can be realized by using this core material in an actual

*Dr. Beiler is Chief Scientist at Westinghouse Aerospace Electrical Division, Lima, Ohio.

inverter application. A comparison of losses for these two materials with 400-cps sinusoidal excitation is given in Figure 1. Since 6-mil "Cubex" material is not yet commercially available, the test data presented in Figure 1 for this material can only be considered representative of the presently available sample quantities. These data show that even non-field-annealed "Cubex" is better than Hipersil at high flux densities. Eleven-mil Hipersil material was chosen for the two identical output transformers because it is readily available in sheet form. Six-mil Hipersil material or data are not readily available for a more direct comparison.

Needed data are presently available for 6-mil "Cubex" material which has been field-annealed. Such data will be taken after the cores are annealed and shall be provided in a following report. This field-annealing process has not been optimized and several procedures will be used to determine the best procedure for reducing core loss.

B. Weight Reduction Through Lamination Configuration.

"E" type cores are commonly used for three-phase sinusoidal voltage transformers and require one-third less core material than would be required for three separate single-phase transformers. This same method of saving magnetic material weight through flux cancellation can be extended, as described on page 66 of Reference 1, for use with a six power-stage static inverter having six square-wave output voltages, phase-displaced 30 electrical degrees from each other.

For this program, a four power-stage static inverter will be used having four square-wave output voltages, phase-displaced 45 electrical degrees from each other. Using harmonic neutralization techniques (see Reference 1 of Appendix V) the secondary windings will be interconnected to produce a three-step, three-phase output voltage with the first harmonic present being the seventh. The basic lamination configuration for this output transformer is shown in Figure 2. Assuming a constant number of turns and wire size, this type lamination requires about 40% less magnetic material than would be required for four separate single-phase transformers.

The fact that the weight of the magnetic material is reduced by using the quadratic transformer rather than using four single-phase transformers, is easily demonstrated. Figures 3 and 4 define the quantities used in the following calculations. The criterion used to determine the cross-sectional area of each core leg is equal peak flux density in all legs.

Let the third dimension of each core be one unit deep; then, the volume of magnetic material in the single-phase transformer is:

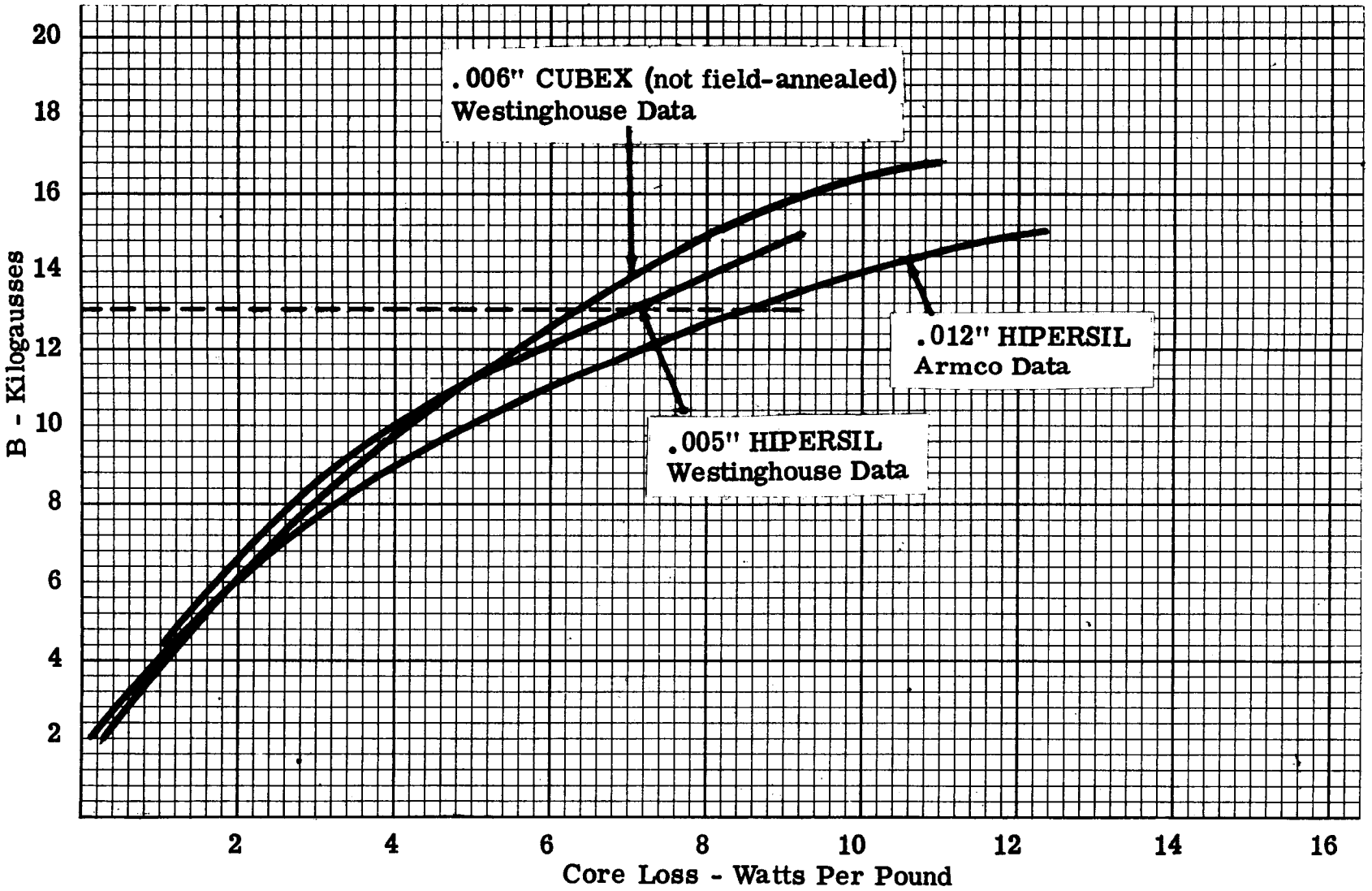


Figure 1. A Comparison of Losses for "Cubex" and "Hipersil" Magnetic Materials with 400-CPS Sinusoidal Excitation

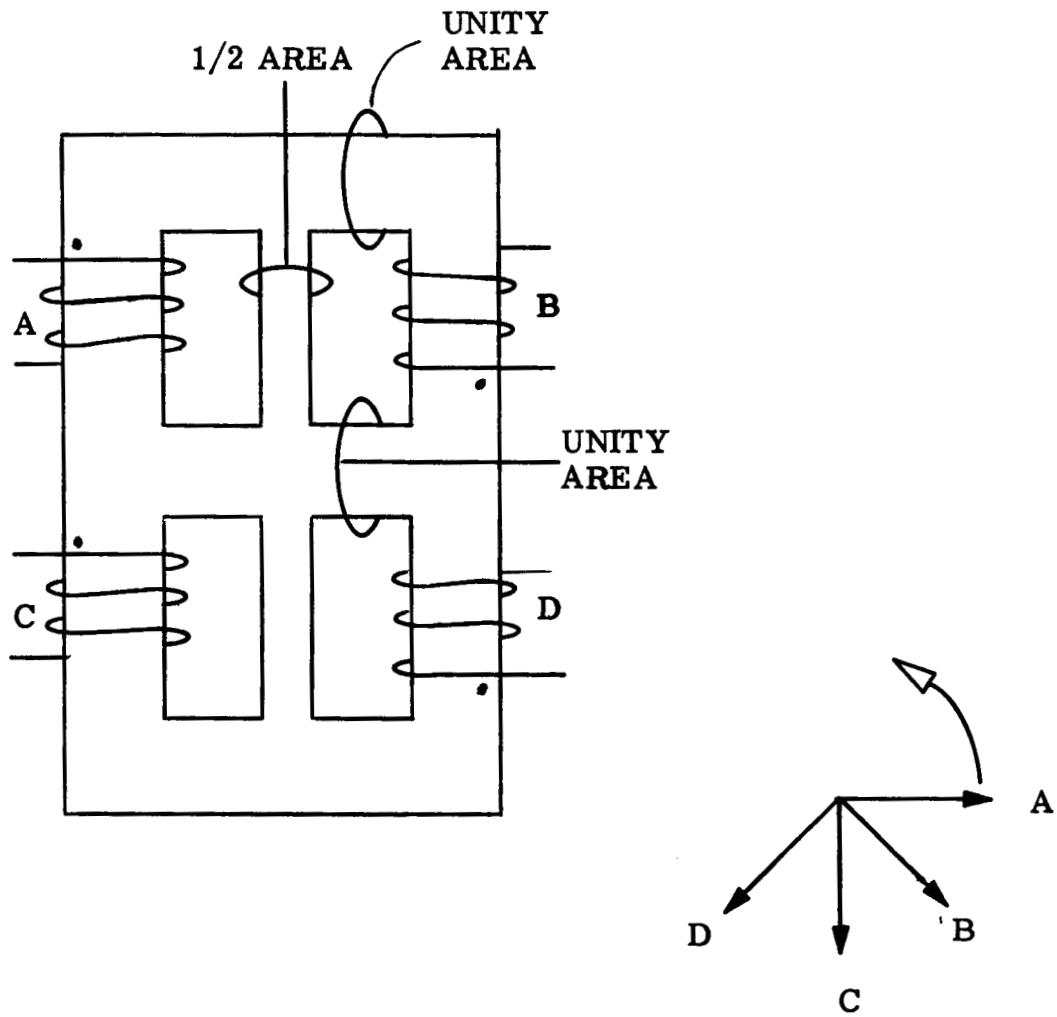
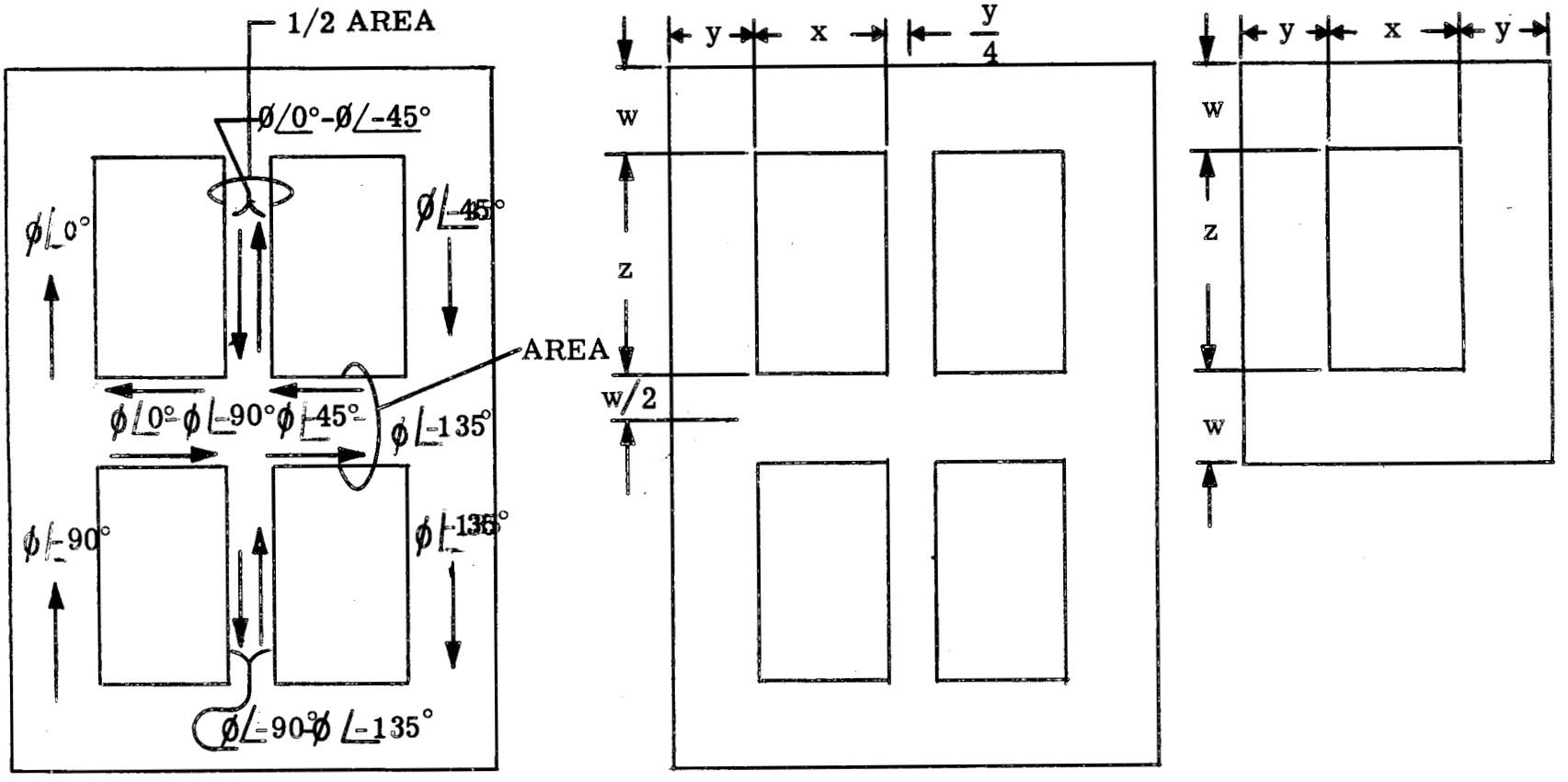


Figure 2. Basic Lamination Configuration for Output Transformer



3a. Flux distribution (fluxes are defined in Figure 4)

3b. Dimensions of quadratic transformer core.

3c. Dimensions of single-phase core.

Figure 3. Definitions of Flux Distribution and Core Dimensions of Output Transformer

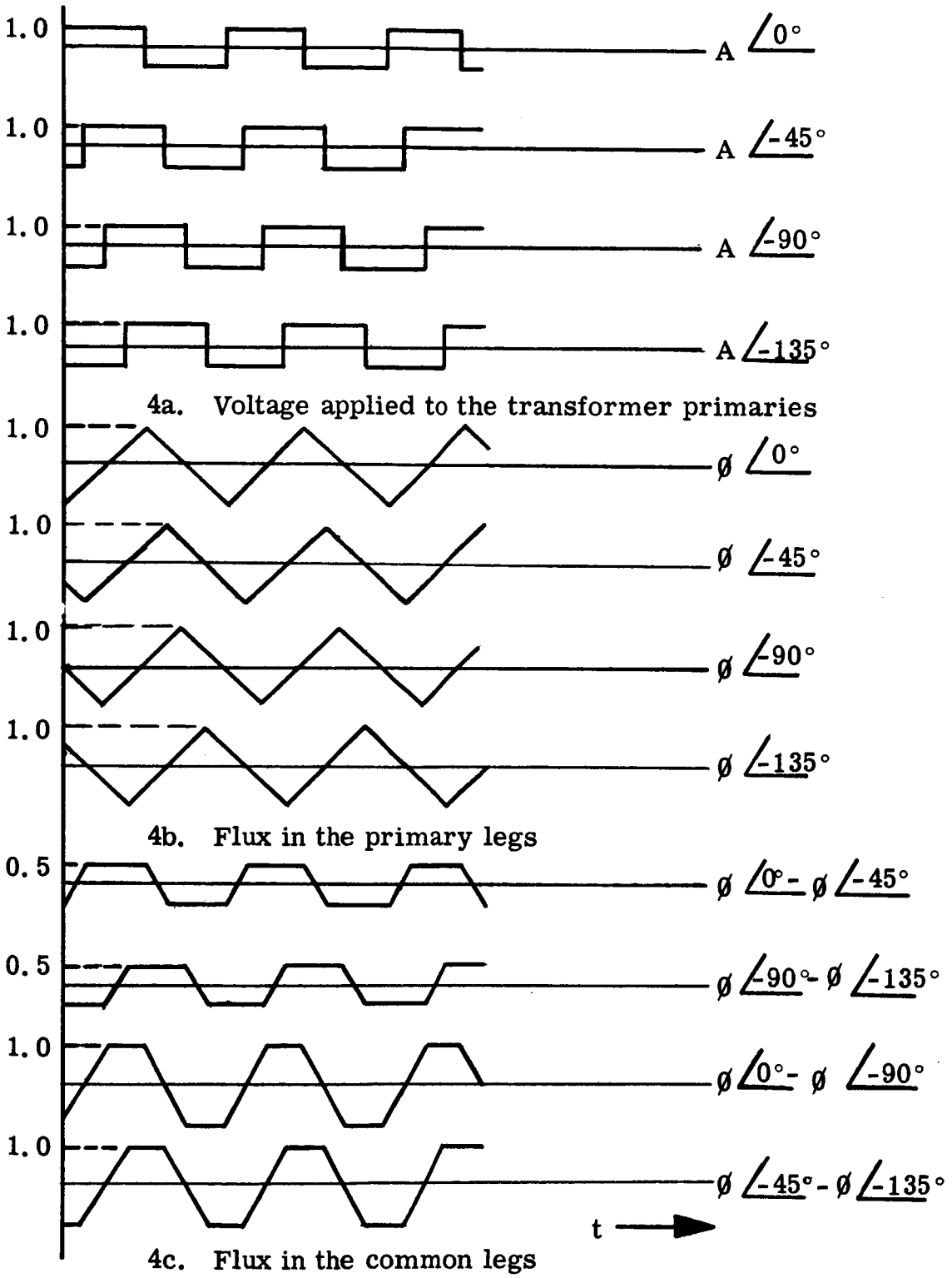


Figure 4. Voltage Applied to the Primary Coils and the Flux Distribution in Each Core Leg

$$U_s = 2\left[wx + yz + wy\right](1).$$

The volume of one-fourth of the quadratic transformer is:

$$\frac{U_q}{4} = \left[\frac{3}{2}wx + \frac{5}{4}zy + \frac{7}{8}wy\right](1).$$

Inspection of U_s and $\frac{U_q}{4}$ shows that U_s is the larger of the two.

Using the maximum actual dimensions of Figures 5 and 6, the volumes are:

$$U_s' = (1.1+3.29+1.1)(.545+.425+.545)-(3.29)(.425)$$

$$= 6.93 \text{ in}^3,$$

and

$$\frac{U_q'}{4} = (1.1+3.29+.6)(.545+.425+.155)-(3.29)(.425)$$

$$= 4.23 \text{ in}^3,$$

The ratio

$$\frac{U_q'}{4U_s'} = \frac{4.23}{6.93} = 0.61.$$

Thus, a weight savings of 39% of the core material has resulted from the use of the quadratic transformer rather than four single-phase transformers.

C. Design of Test Transformer.

To facilitate machine winding of the four transformer coils and to permit use of available tooling for punching the laminations, the actual lamination configurations which will be used are shown in Figures 5 and 6. Placing two of the short laminations in between each layer of long laminations results in a core having the basic lamination configuration of Figure 2. By alternating the gaps between ends of the short laminations from one side of the core to the other, the long laminations will carry 33% more flux than usual in the area of these gaps. This staggered gap is designed to produce the "hermaphroditic" effect discussed on page 65 of Reference 1. This effect is useful in reducing the saturation current spikes which normally result from "ratcheting up" the magnetic hysteresis loop. This staggered gap accomplishes, with greatly reduced loss, the effect of gapping the whole core cross-section in output transformers.

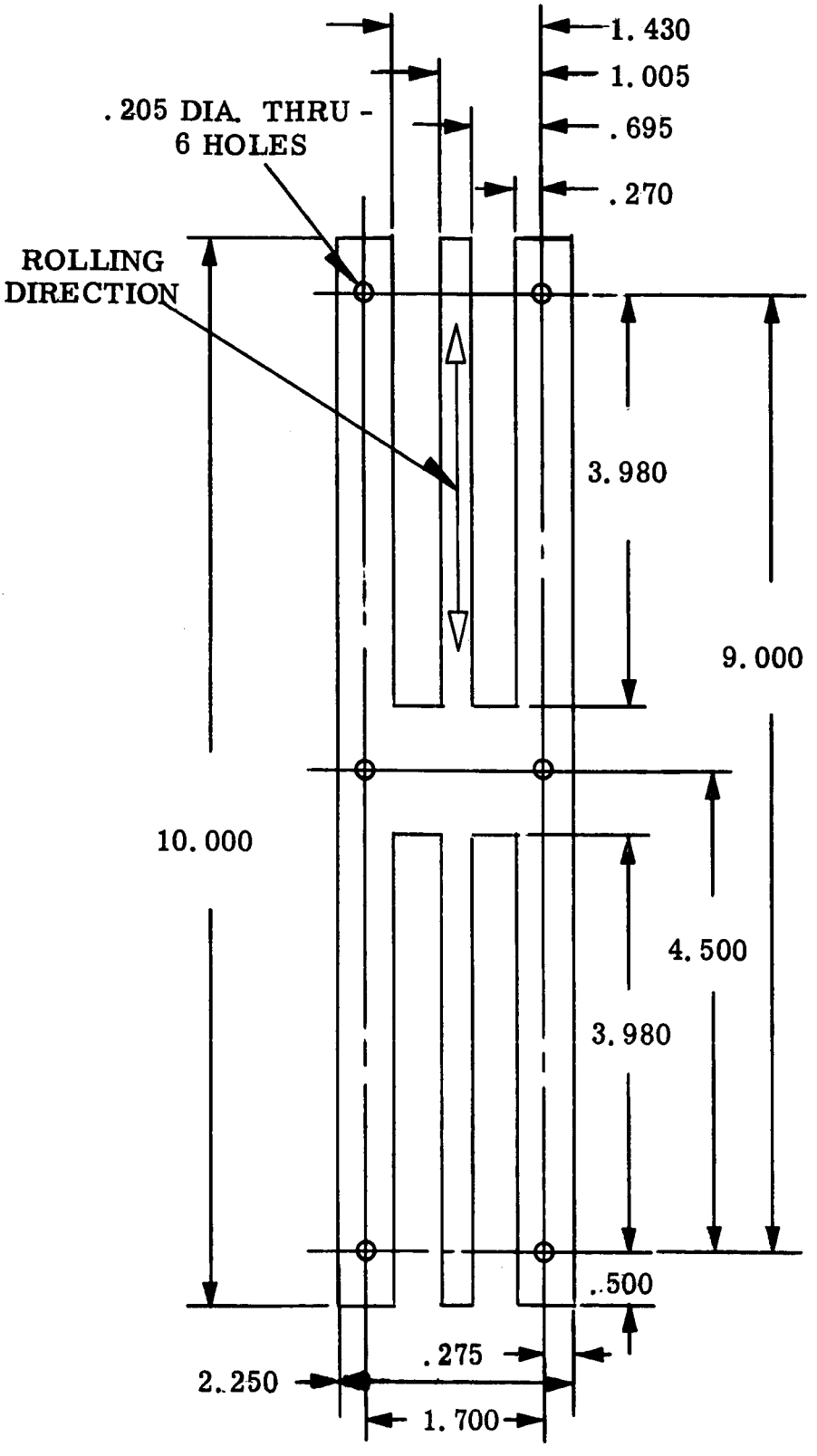


Figure 5. Actual Output Transformer Long Lamination Dimensions

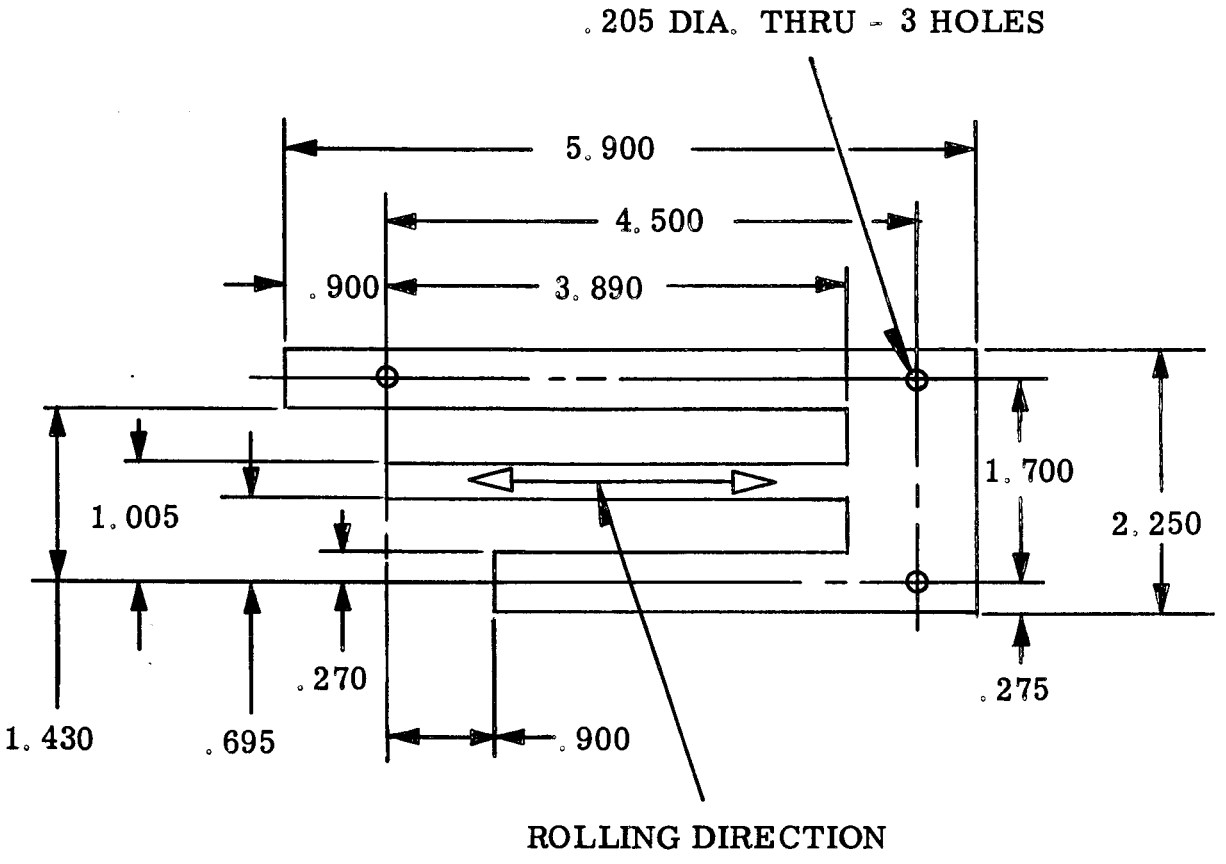


Figure 6. Actual Output Transformer Short Lamination Dimensions

The turns and core cross sectional area were designed to produce a maximum flux density, B_m = 13 kilogauss. With a nominal volts/turn of 0.7, the required stack height is approximately 0.95 inch. Figure 1 shows that Cubex iron has a core loss of 6.3watts per pound while .012 Hipersil iron has a core loss of 8.5 watts per pound at 13 kilogauss excitation.

The nominal rating of the transformer is 750 VA and its calculated weight is 6.9 pounds, excluding leads. Figure 7 is a schematic diagram of the output transformer and gives the turns and winding interconnections required to produce a three-phase, 115-volt output with the third and fifth harmonics neutralized. Appendix V shows the relation of the output transformer to the entire inverter.

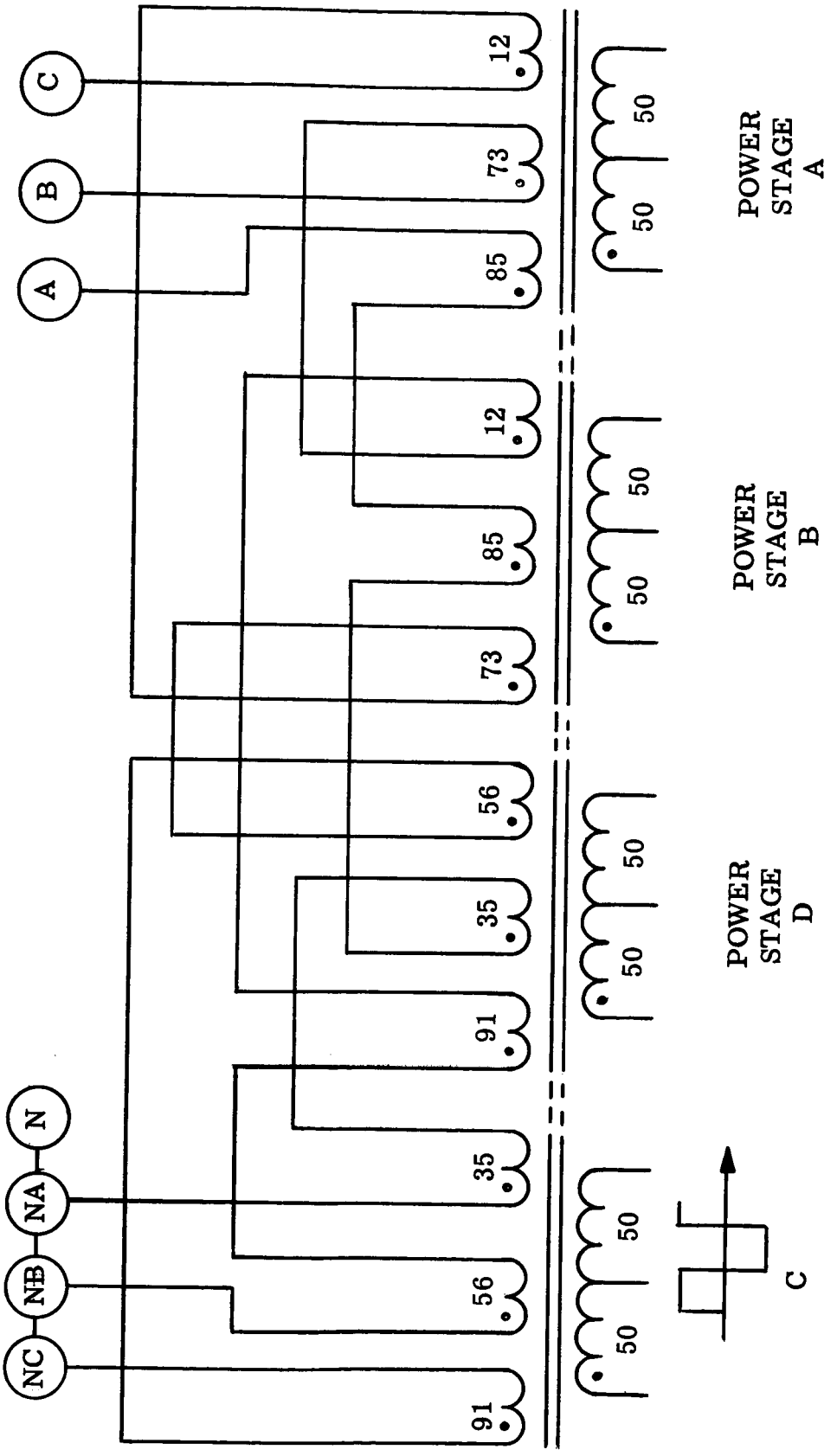


Figure 7. Output Transformer Schematic Diagram
(Numbers Indicate Turns)

IV. CONSIDERATIONS FOR PARALLELING STATIC INVERTERS

A. Mathematical Analysis.

1. Load Sharing Control Method.

Successful operation of a system consisting of two or more inverters supplying a common bus requires that the total system load be divided nearly equally among the parallel inverters. In the event of unequal load sharing, the problem is to sense or detect the cause or causes and to initiate the proper corrective actions. This is accomplished in the case of paralleled alternators by sensing real and reactive power. Any change in the average real power of an alternator must be accomplished by changing the governor or control on its prime mover. The reactive load is then adjusted by changes in excitation. There seems to be no such inherent separation of functions in the present type static inverter.

An analysis based on a Thevenin's equivalent circuit approach (Equations (23) and (24) derived in Appendix I and repeated below) indicates that, for inverters, an unbalance in reactive load does not necessarily result from a difference in voltage magnitudes. Likewise, an unbalance in real load does not necessarily result from a difference in phase.

$$(23)\quad R(\dot{I}_1-\dot{I}_0)\tilde{=}\frac{\Delta E}{Z_1}\cos(\theta_0-\theta_1)-\frac{E_0\Delta\theta}{Z_1}\sin(\theta_0-\theta_1)$$

$$(24)\quad Q(\dot{I}_1-\dot{I}_0)\tilde{=}\frac{\Delta E}{Z_1}\sin(\theta_0-\theta_1)+\frac{E_0\Delta\theta}{Z_1}\cos(\theta_0-\theta_1)$$

where $R(\dot{I}_1-\dot{I}_0)$ = The component of unbalanced current that is in phase with the bus voltage.

$Q(\dot{I}_1-\dot{I}_0)$ = The component of unbalanced current that is in quadrature with the bus voltage.

E_0 = Magnitude (rms) of internal voltage if it was adjusted so that differential current was zero.

θ_0 = Angle (with terminal voltage as reference) of internal voltage if it was adjusted so that differential current was zero.

$\dot{Z}_1 = Z_1\angle\theta_1$ = Internal impedance of voltage source.

ΔE, $\Delta\theta$ = Incremental quantities.

The controlling factor is the angle $(\theta_o-\theta_1)$. Since the angle θ_o is a function of both the internal impedance and load impedance, these two impedances are the controlling factors. (See Appendix I, Equation 14) .

If $(\theta_o-\theta_1)\tilde{=} -90°$, Equations (23) and (24) become

(23a) $$R(\dot{I}_1-\dot{I}_o) = \frac{E_o}{Z_1}\,\Delta\theta$$

(24a) $$Q(\dot{I}_1-\dot{I}_o)\tilde{=} -\frac{\Delta E_o}{Z_1}$$

and a real component would indicate phase difference and a reactive component would indicate a magnitude difference.

If $(\theta_o-\theta_1)\tilde{=} 0°$, Equations (23) and (24) become

(23b) $$R(\dot{I}_1-\dot{I}_o)\tilde{=}\frac{\Delta E_o}{Z_1}$$

(24b) $$Q(\dot{I}_1-\dot{I}_o)\tilde{=}\frac{E_o}{Z_1}\,\Delta\theta$$

and the exact opposite is indicated.

If $(\theta_o-\theta_1) = -45°$, Equations (23) and (24) become

(23c) $$R(\dot{I}_1-\dot{I}_o)\tilde{=} .707\,\frac{(\Delta E+E_o\Delta\theta)}{Z_1}$$

(24c) $$Q(\dot{I}_1-\dot{I}_o)\tilde{=} .707\,\frac{(E_o\,\Delta\theta-\Delta E)}{Z_1}$$

and therefore, the real or the reactive component could be a result of a difference in magnitude and/or phase.

If $\theta_1\tilde{=} 90°$, that is, the internal impedance of the inverter is practically a pure inductance, and if θ_o is small, Equations (23a) and (24a) indicate that the internal phase should be controlled by sensing differential real current and the magnitude of the internal voltage should be controlled by sensing differential reactive current.

In practice, it might not be practical to make the internal impedance purely inductive or purely resistive. (A pure resistance would make

Equations (23b) and (24b) hold.) However, in Appendix I it is shown that the In-Phase component of (I_1-I_0) with a phasor θ_2 degrees ahead of the corresponding terminal voltage is given by:

$$(23d) \quad R_{\theta_2}(\dot{I}_1-\dot{I}_0)\tilde{=} \frac{\Delta E}{Z_1} \cos(\theta_0-\theta_1-\theta_2) - \frac{E_0\Delta\theta}{Z_1} \sin(\theta_0-\theta_1-\theta_2)$$

and the In-Quadrature component is given by:

$$(24d) \quad Q_{\theta_2}(\dot{I}_1-\dot{I}_0)\tilde{=} \frac{\Delta E}{Z_1} \sin(\theta_0-\theta_1-\theta_2) + \frac{E_0\Delta\theta}{Z_1} \cos(\theta_0-\theta_1-\theta_2).$$

If equations similar to Equations (23a) and (24a) are to hold for this case:

$$(25) \quad \theta_0-(\theta_1+\theta_2)\tilde{=} -90° \text{ or } (\theta_1+\theta_2)\tilde{=} 90 + \theta_0.$$

Therefore, if the internal impedance is not purely inductive, it can be compensated for by using a reference phasor that leads the terminal voltage θ_2 degrees, such that:

$$(26) \quad \theta_2\tilde{=} 90° + \theta_0 - \theta_1.$$

This leading phasor could be one of the line-to-line voltages if $\theta_2 = 30°$ or another line-to-neutral voltage if $\theta_2 = 60°$. It could be determined by phase shifting any of the voltages.

If it is assumed that differential current sensing and comparing are provided in such a manner as to make Equations (23d) and (24d) hold, there are two basic methods of parallel control.

Method 1:

Lock the oscillators to assure frequency lock. Since it is possible to have the frequencies of the internal voltages the same but be out of phase, some method of assuring that the internal voltages are in phase must be provided. With the "front-ends" locked, means for "quadrature" current control based on Equations (23d) and (24d) with $\Delta\theta$ set equal to zero could be provided.

Method 2:

In this method there are no cross ties between "front-ends" of the inverters. This type of control would be very similar to that now used in alternator systems. Differential current sensing and comparing are achieved in the same manner as in Method 1. The quadrature com-

ponent would again control the magnitude. However, the in-phase component would control the frequency directly. Changes in phase would be accomplished by changing the frequency for a small interval of time.

Method 1 will be the method used in the experimental work because it requires less complex control circuits, it is more readily adapted to existing inverter circuits, and it does not interfere with precise frequency requirements. If the reference phasor is picked such that

$$\theta_0 - \theta_1 - \theta_2 \tilde{} = 90°$$

and if one of the inverters has an internal voltage greater than the average, it will result in that inverter taking more lagging reactive current (in reference to a voltage θ_2 degrees ahead of the phase voltage in which the differential current loop is placed) than the average and its reactive load division circuit would need to reduce the "excitation" voltage of that inverter. θ_0 is related to the internal impedance by the following equation:

$$(18) \quad \operatorname{Tan}\theta_0 = \frac{\sin(\theta_1 - \Psi)}{\frac{2Z_{Lp}}{Z_1} + \cos(\theta_1 - \Psi)}.$$

Therefore, if Z_1 is known, a proper value of θ_2 may be determined.

2. Sensing Circuit Gain Calculation.

The "open loop" relation for internal voltage is derived in Appendix II and given below:

$$(33) \quad \Delta E = (V_{pL} - V_{1L}) \frac{\partial E}{\partial V_s} + \left|\frac{\dot{Z}_1 + \dot{Z}_L}{Z_L}\right| (V_{1L} - V_o) + \frac{\partial E}{\partial I_{DQ}} (\Delta I_Q).$$

The voltage regulator gain, $\frac{\partial E}{\partial V_s}$, can be calculated from the single-unit circuitry or if one has knowledge of the single-unit, closed-loop regulation it can be calculated by use of the following formula:

$$(34) \quad \frac{\partial E}{\partial V_s} = \frac{V_{N.L.} - \left|\frac{\dot{Z}_1 + \dot{Z}_L}{Z_L}\right| V_{F.L.}}{V_{N.L.} - V_{F.L.}}$$

If Z_1 and V_{1L} are known, (assume $V_{pL} = V_o$), Equations (33) and (24d)

can be solved simultaneously for parallel control circuit gain, $\frac{\partial E}{\partial I_{DQ}}$, for a given load and allowable differential current, ΔI_Q.

Therefore:

$$(35) \qquad \frac{\partial E}{\partial I_{DQ}} = \frac{Z_1}{\sin(\theta_o - \theta_1 - \theta_2)} - \left[\frac{(V_{pL} - V_{1L}) \frac{\partial E}{\partial V_s} + \left| \frac{\dot{Z}_1 + \dot{Z}_L}{Z_L} \right| (V_{1L} - V_{pL})}{\Delta I_Q} \right].$$

3. Internal Impedance Calculation and Its Use.

It will be observed that in order to make use of the relationships stated above, the internal impedance, $\dot{Z}_1$, must be known. If balanced loads are assumed the equivalent circuit, on a per phase basis, for calculating the internal impedance is shown in Figure 8. The impedance looking back into the series-connected secondaries in phase one is Z_{eq}. In Appendix III an equation is developed for determining Z_{eq}. (Equation (75)). With Z_{eq} known, the internal impedance of the inverter can thus be calculated by substituting values in the circuit of Figure 8 and making a few series-parallel transformations.

In Appendix I V the internal impedance of the static inverter models, which will be used in this program, is calculated and is $\dot{Z}_1 = 0.27$ P. U. $\angle 77.8°$. The required inverter voltage gain is calculated using this internal impedance and voltage regulation limit of 115 ± 0.7 volts and is $\frac{\partial E}{\partial V_s} = -38$.

By assuming an initial full load voltage setting accuracy of 115 ± 0.2 volts, and a load division accuracy of 10%, the required gain of the reactive load-division-circuit is calculated in Appendix I V and is $\frac{\partial E}{\partial I_{DQ}} = -0.412$ where E and I_{DQ} are in per unit values.

B. Circuit Development.

1. Frequency & Phase Locking Circuits.

Using the paralleling method chosen for this study, the frequency and phase must be the same on all sources prior to connecting them in parallel. Therefore, all inverters to be paralleled must operate from the same frequency reference and be locked in phase with each other.

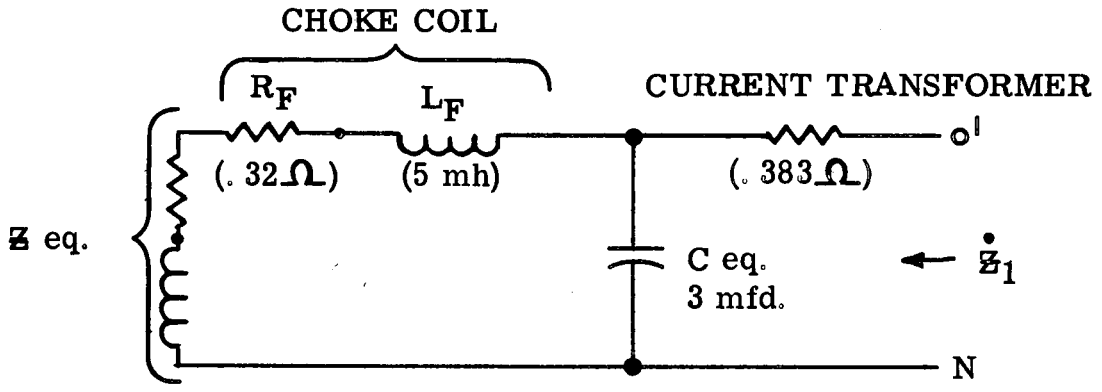


Figure 8. The Equivalent Circuit for Internal Impedance of a Static Inverter Under Balanced Load Conditions

For increased reliability, each inverter must be capable of operating independently or in parallel with similar inverters. To operate independently means that each inverter must have its own frequency reference. The requirement that they operate in parallel with similar inverters means that all inverters must obtain their frequency reference signal from a single reference. Thus, some means must be derived to remove all but one frequency reference signal and connect that frequency reference signal to all inverters whenever parallel operation is desired.

The only practical way that was devised to accomplish the above objectives is shown in Figures 9 and 10. See Appendix V. When inverter #1 is operating independently, switches S1 through S5 are open (Figure 9). Transistor Q24 is normally on (i. e., driven into saturation). Its base current is delivered by resistor R62. The tuning fork oscillator (TFO1) provides a 3200 pulse per second signal to trigger a Unijunction Transistor Relaxation Oscillator (UTRO), which provides pulses for operating the countdown circuit of Figure 10. The operation of countdown flip-flops is described in Reference 1. An addition to the countdown circuit described in the above reference is an inhibit circuit employed to ensure that the only possible stable state for the countdown flip-flops is the one that provides proper phase sequence of the inverter output voltage. This inhibit circuit consists of R49, R50, CR89, 90 and 91. The paths provided by those components ensure that Q18B, Q18C, and Q18D are on before Q18A can be turned off by a signal from the UTRO. The signal from the UTRO varies from about 10 volts positive to 0 volts with respect to ground at a 3200 pps rate. The countdown flip-flops change state only under certain conditions. One of these conditions is that the signal from the UTRO must be zero. The other condition is that the capacitor (C16 or C17) in series with the base of the transistor to be shut off, must be charged positive with respect to ground so the base current can be diverted to ground. If the countdown flip-flops start in the correct sequence, each flip-flop can change states every fourth zero from the UTRO, i. e. one flip-flop changes state during one UTRO pulse. If the countdown circuit does not start in the correct sequence, then either Q18B, Q18C or Q18D will be off when Q18A is set up to be shut off. Therefore, CR42A will be reverse biased by the collector voltage of either Q18B, Q18C or Q18D so that Q18A cannot be shut off. When Q18A is on, Q17A is off. The collector voltage of Q17A charges Q17B through R48B, C16B, R47B and Q18A negative with respect to ground so that once Q18B is turned on it cannot be turned off by a pulse from the UTRO. Q18C and Q18D have similar conditions set up in C - D sequence. When Q18B, Q18C, and Q18D are on, Q18A can be shut off by the next UTRO signal. The correct phase sequence is now set up.

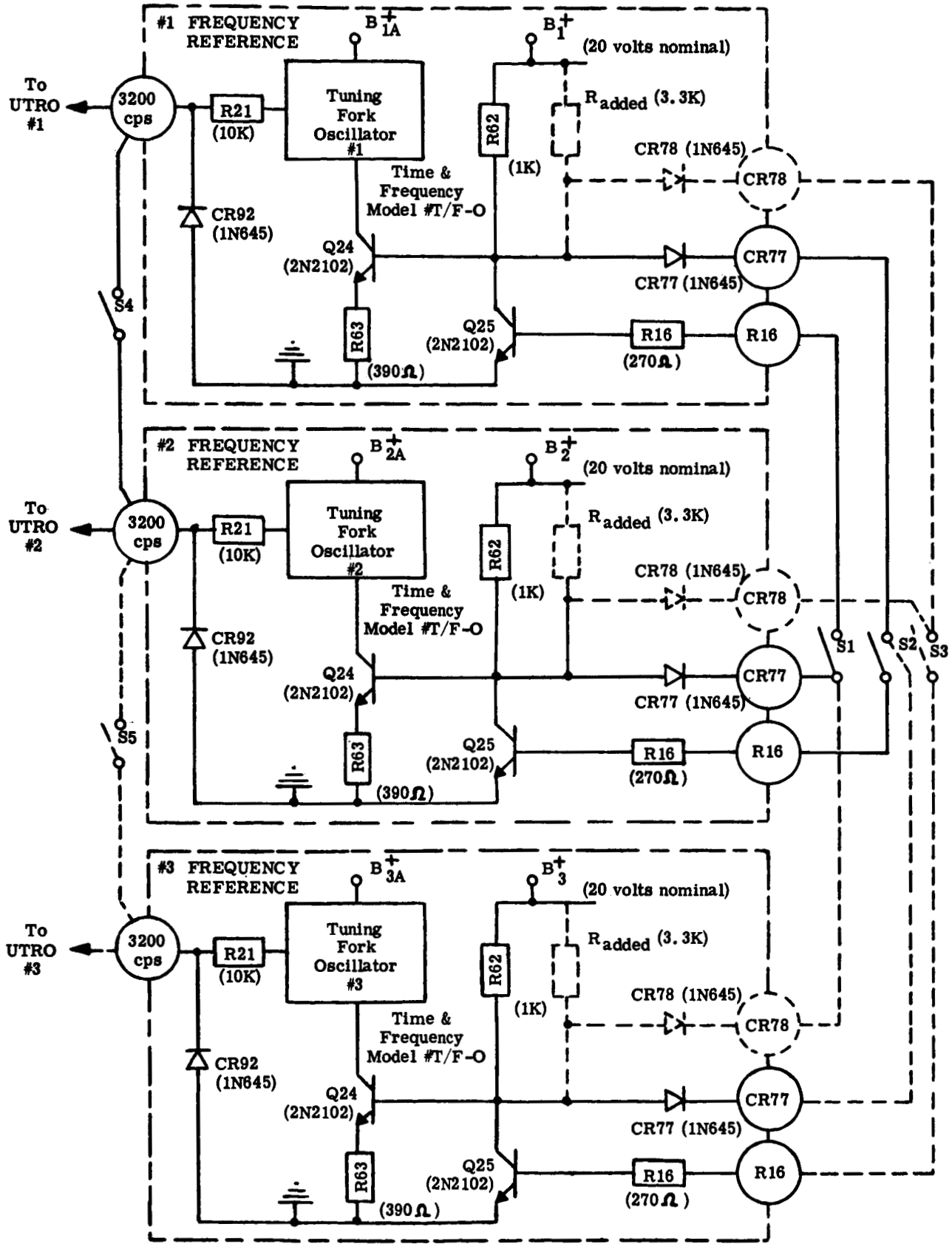


Figure 9. Frequency Locking Circuits
(Solid interconnections show two units paralleled; Solid and dotted interconnections show three units paralleled.)

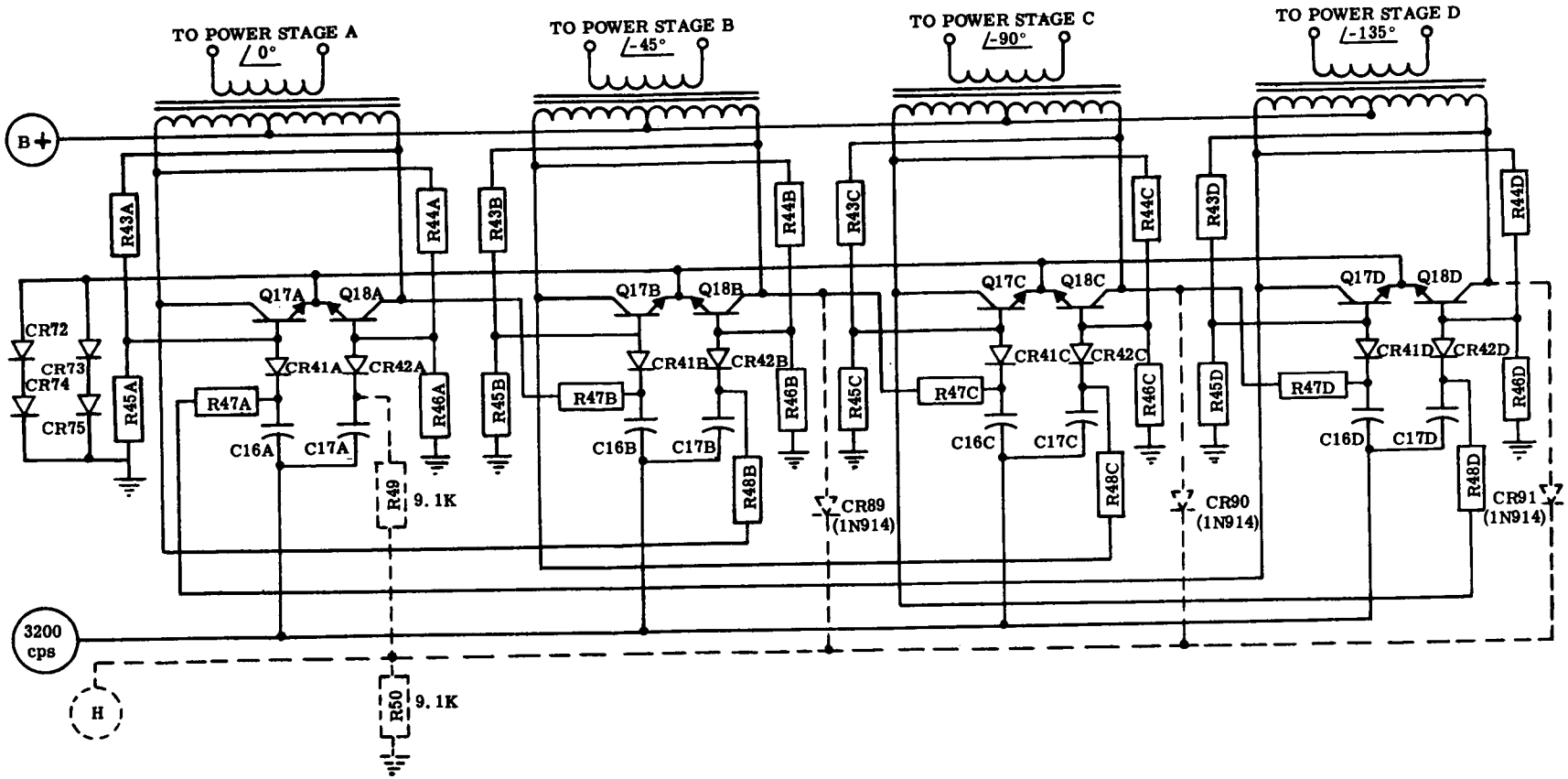


Figure 10. Schematic Diagram of a Typical Countdown Circuit with Phase Locking Provisions
(The dotted components ensure proper phase locking)

By connecting the (H) terminals (Figure 10) of all inverters to be paralleled together, all inverters will operate in phase with each other. Of course, all inverters must be operating at the same frequency prior to making that connection since the phase of all inverters cannot be the same if they are operating at different frequencies.

The method that is proposed to accomplish the removal of all but one frequency reference signal and to connect that frequency signal to all inverters to be paralleled is based on the assumption that any of the frequency references on any of the inverters to be paralleled will operate within the frequency accuracy required. The circuit shown in Figure 9 is designed to arbitrarily select one of two references in the following manner. With switches S1, S2 and S4 closed, d-c voltage is applied to both inverters. The UTRO's of both inverters will free run at different frequencies until a frequency reference is selected. Transistor Q24 on one of the inverters and transistor Q25 on the other inverter will turn on due to unbalance in the bistable circuit involved. Assume that Q24 on inverter #1 and Q25 on inverter #2 turn on first. Then R62 of inverter #1 will supply base drive for Q24 on inverter #1 and Q25 on inverter #2. Consequently, Q25 on inverter #2 will divert base drive away from Q24 on inverter #2 and Q25 on inverter #1 to ground. TFO #1 will operate but TFO #2 will not operate. The operating TFO will supply its frequency signal to both UTRO's so both inverters will operate at the same frequency. If Q24 on inverter #2 and Q25 on inverter #1 turn on first, then replace all #1 by #2 and #2 by #1 above. Now the (H) terminals on both inverters can be connected to provide correct phase lock.

Three or more units are paralleled in a similar manner. The interconnections to parallel three units are shown dotted on Figure 9. It should be noted that for every inverter added to the bus, a diode (CR78) and resistor (3.3K) shown dotted in Figure 9, must be added to all inverters. This diode and resistor supply base current for the added frequency reference. Also, if only two inverters are to be paralleled, then CR77 can be replaced by a short circuit.

This circuit selects one frequency reference immediately after d-c voltage is applied to the inverters. The connection of all (H) terminals together must be delayed until that one frequency reference is operating. With the tuning fork oscillators selected for the inverter models, this delay will be from three to five seconds. If an instant starting type frequency reference were used (i.e., crystal oscillator, multivibrator, etc.), this delay would be unnecessary.

2. Load Division Circuit.

As shown in Appendix IV, the "reactive" load division circuit for the static inverters, which will be paralleled in this study, should have a gain as follows:

$$\frac{\partial E}{\partial I_{DQ}} = -0.412$$

for differential load currents which lag the phase voltages by 60 degrees. This means that if an inverter were supplying a current equal to 1 P.U. $\angle -60°$ more than the average phase current supplied by each inverter, then the load division circuit should be capable of causing the inverter output voltage to drop 0.412 P.U. to 67.5 volts line-to-neutral. Figure 11 illustrates the desired response of this circuit.

The a-c load division circuit designed for this purpose is shown in Figures 12 and 27 and is an adaptation of techniques used in voltage regulators for a-c parallel generator systems. The voltage reference in this circuit consists of two 43.4 volt zener diodes (CR55 and CR56) connected in a bridge which balances with 86.8 volts applied and has a nominal d-c current requirement of 15 milliamperes. When load is divided perfectly, there is no circulating current through R64, 65, 66 and C21 from the load division sensing current transformer (T27) and all voltage and current for balancing the voltage reference bridge is supplied by the voltage sensing transformer (T29) through the full wave rectifiers (CR51, 52, 53, 57, 58 and 59) and the voltage adjusting resistor R15.

Transformer T28 consists of two separate 2:1 step-down transformers which are used for impedance transformation and to provide isolation. A common value of 1 microfarad was chosen for C21. Resistors R65 and R66 are adjusted so that the voltage across the series combination lags the 400-cps current through it by 60 electrical degrees.

$$R65+R66 = \frac{X_{C21}}{\tan 60°} = \frac{1}{2\pi 400 \times 1 \times 10^{-6} \times \sqrt{3}} = 230 \text{ ohms.}$$

The voltage across R64 will be in phase with the current through it. To keep the voltage across R64 equal to the voltage across the R65, R66 and C21 combination, the impedance of R64 must be the same as the impedance of the RC combination.

$$R64 = \sqrt{(R65+R66)^2+(X_{C21})^2} = \sqrt{(230)^2+(398)^2} = 460 \text{ ohms.}$$

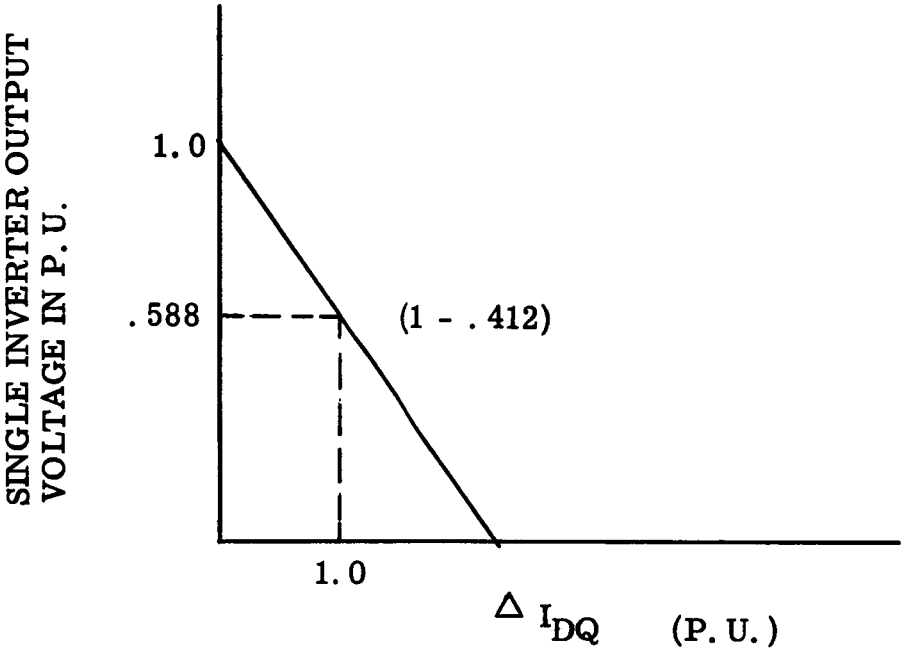


Figure 11. Desired Transfer Curve for the AC Load Division Circuit

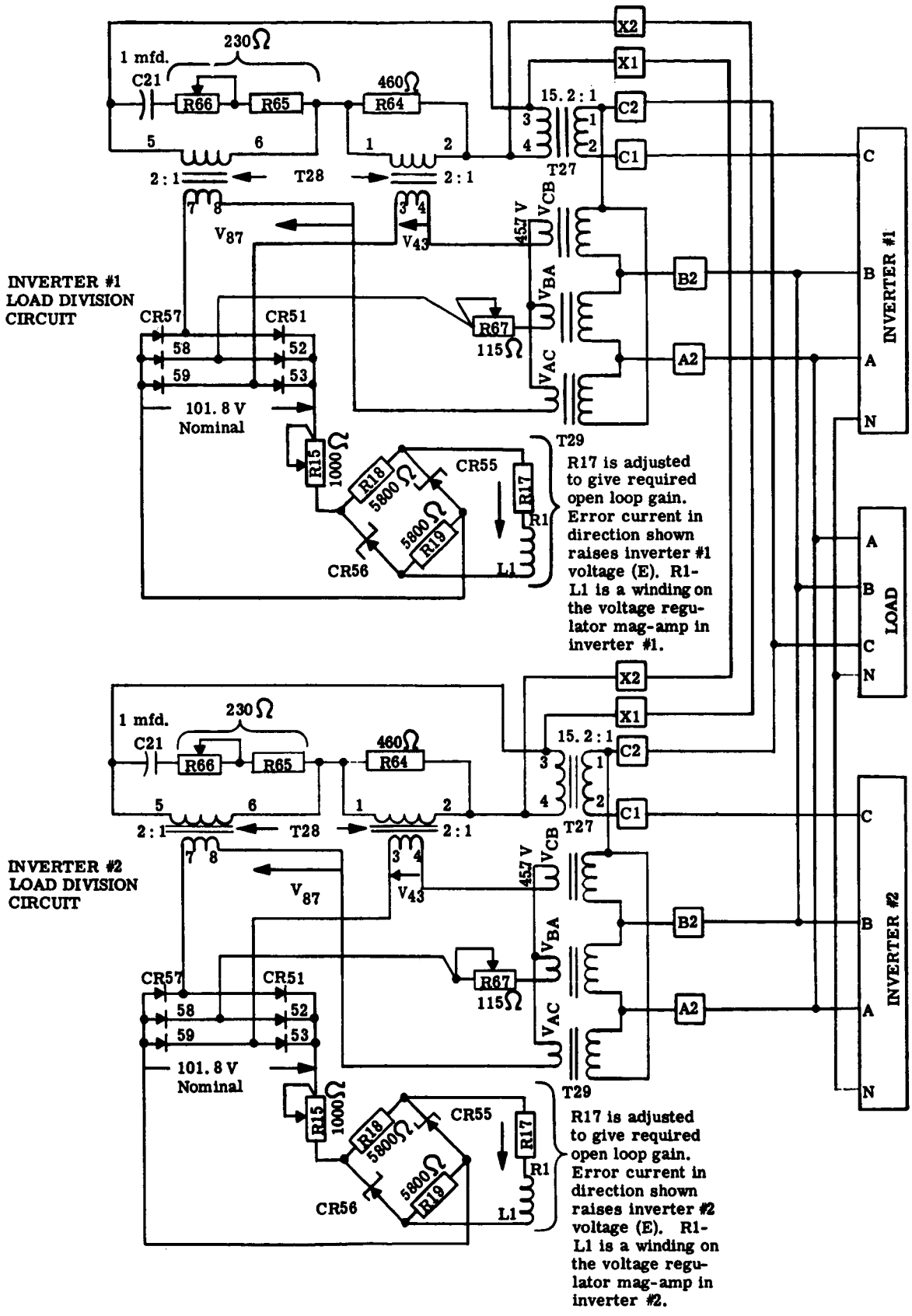


Figure 12. Two Inverter Block Diagrams Connected in Parallel with AC Load Division Circuits Shown

The impedance presented by the secondaries of transformer T28, under conditions of perfect load division, is approximately equal to the turns ratio squared times the primary impedance:

$$(1/2)^2 \text{ X } 460 = 115 \text{ ohms.}$$

To present balanced voltages to the three-phase bridge rectifier (CR51, 52, 53, 57, 58 and 59) resistor R67 will be set at approximately 115 ohms.

By assuming that R15 is nominally set at 1000 ohms, the required secondary voltage of T29 was determined as follows: The d-c voltage required out of the full wave bridge rectifier equals the nominal voltage reference level (86.6 volts) plus the nominal voltage drop across R15 (1K x 15 ma = 15 volts) making a total of 101.8 volts. The required line-to-neutral voltage and current into the full wave bridge rectifier were determined by the usual bridge rectifier characteristics.

$$I_{ac} = 15 \text{ ma x } .816 = 12.24 \text{ ma,}$$

$$E_{LN} = \frac{0.74 \text{ x } 101.8 \text{ volts} + 2 \text{ x } 0.7}{\sqrt{3}} = 44.3 \text{ volts.}$$

Transformer T29 must supply this voltage plus the voltage drops from the secondaries of T28 and R67 which gives (44.3 volts + 0.0124 amps x 115 ohms) a total secondary voltage of 45.7 volts. Therefore, T29 was designed to provide 45.7 volts output per phase with 200 volts input per phase.

To determine the required turns ratio of the load division current transformer (T27), it was assumed that X1 and X2 were disconnected and that the inverter was supplying an output current of 1 P.U $\angle -60°$ = 2.18 amps $\angle -60°$. Under these conditions, the inverter output voltage should be caused to drop to 67.5 volts line-to-neutral by the voltages introduced in the sensing circuit transformer T28. By knowing these secondary voltages, the primary voltages (T28) and the required secondary current of T27 can be determined. Figure 13 is a phasor diagram of this circuit under these conditions with phase C voltage taken as the reference phasor. The secondary voltages of T29 (V_{CB}, V_{BA}, and V_{AC}) will have a magnitude of 26.8 volts $(45.7 \text{ x } \frac{67.5}{115})$. Temporarily neglecting the voltage drop across R67, the voltages required from T28 (V_{43} and V_{87}) must have a magnitude of 30.4 volts:

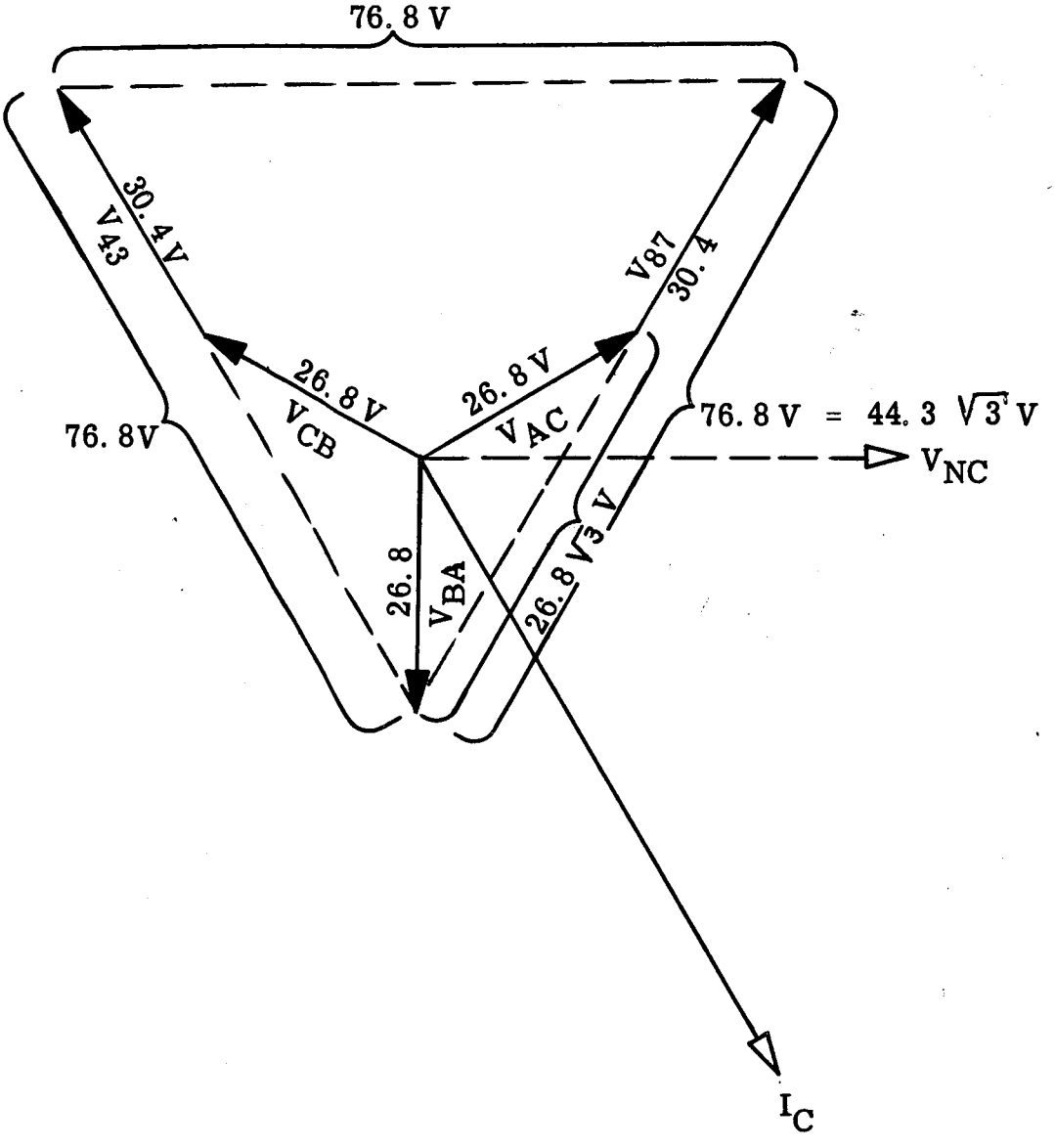


Figure 13. Phasor Diagram of AC Load Division Circuit with a Differential Load Current of 1 PU ∠-60°

$$|V_{87}| = |V_{43}| = 44.3 \times \sqrt{3} \text{ (line-to-line voltage required into bridge rectifier)}$$
$$- 26.8 \times \sqrt{3} \text{ (line-to-line voltage from T29)} = 30.4 \text{ volts.}$$

The voltage drop across R67 (0.0124 amps x 115 ohms = 1.4 volts) subtracts from V_{BA} and is compensated for by increasing both V_{43} and V_{87} by the vectorial equivalent amount of 0.8 volts $\left(\frac{1.4 \text{ volts}}{2 \cos 30°} = 0.808 \text{ volts}\right)$. Therefore, the desired secondary voltages of T28 under this unbalanced condition are 30.4 + 0.8 = 31.2 volts.

The current through R64 to obtain the required primary voltage is:

$$I_{R64} = \frac{V_{43} \times 2}{R64} = \frac{31.2 \times 2}{460} = 0.136 \text{ amps.}$$

The current through the transformer primary (T28) is equal to the secondary current divided by the turns ratio $\left(\frac{0.01224 \text{ amps}}{2} = .00612\right.$ amps) plus a small transformer exciting current. These currents are small compared to I_{R64} and will be provided for by letting I_{CT} = 1.05 x I_{R64} = 1.05 x 0.136 = 0.143 amps with one per unit primary current.

The required turns ratio of the load division transformer (T27) can now be determined:

$$\text{Turns ratio (T27)} = \frac{1 \text{ P.U.}}{0.143 \text{ amps}} = \frac{2.18}{0.143} = 15.2 .$$

Current transformer T27 will be wound with this turns ratio.

The above example calculations were for the purpose of designing the load division circuit with sufficient gain to assure load division within 10%. The phasor diagram of Figure 13 is for a load unbalance 10 times this amount. Other phasor diagrams could be drawn to illustrate operation under more typical unbalance load conditions. In actual parallel operation, I_C (Figure 13) can be considered the differential current and may lead or lag V_{NC} by any angle from 0° to 90°. This load division circuit is most sensitive to differential currents which lead or lag V_{AC} by 90°.

During parallel operation of the two model inverters, X1 from one inverter will be connected to X2 of the other inverter and vice versa. (Any number of inverters could be connected in this loop.) In this manner, the current which circulates in these interconnecting wires is proportional to the average current supplied by both (all) inverters, and the CT current which circulates through R64, 65, 66, and C21 is proportional to the differential current. This differential current is the difference between the actual current delivered by one inverter and the average current delivered by all inverters. The operation of this load division circuit always tends to reduce this differential current toward zero.

V. CONSIDERATIONS FOR PARALLELING STATIC CONVERTERS

A. Load Sharing Control Method.

Load sharing between paralleled converters can be accomplished by adjusting the internal voltage of each converter as a function of differential load current. The output current of each converter must be sensed and compared to the average output current of all paralleled converters. The interval voltage of each converter should be automatically adjusted to give proper load division. The proper load division ratio for each converter is determined by the ratio of the KW rating of the individual converter to the sum of the KW ratings of all paralleled converters. This study is concerned with paralleling similar converters, so each converter should supply an equal current.

The circuit that is proposed to accomplish proper load division of paralleled converters is shown in Figures 14 and 27. Transductor T30 is a simple saturable reactor (Reference 3) which senses the d-c current of the converter and applies a signal to the full wave bridge consisting of CR85 through CR88. The output of T30 should be linear with respect to the output current at least up to 1.25 P. U. current. All T30's on the other paralleled converters should have the same characteristics so that there will be no current flowing in the L2-R2 windings when balanced load conditions exist. Transformer T31 supplies a-c voltage for T30. Resistor R69 is adjusted to give 20 volts d-c from the full wave bridge at 1 P. U. load current, The L2-R2 winding is a control winding on a magnetic amplifier in the inverter which causes the internal voltage to be raised or lowered. Current in the direction of the arrow will cause the converter A internal voltage to decrease and the internal voltage of converter B to increase. The direction and magnitude of the current in the control winding are determined by the relative output current magnitudes of the respective converters.

Any number of converters could be paralleled by connecting them to the load bus and the Y1-Y2 terminals.

B. Circuit Design Calculations.

The design of T30 and selecting the value of resistor R70 in series with the L2-R2 control winding were based on a maximum allowable current unbalance of 10% at 1 P. U. load. The voltage across R69 is to be set at 20 volts at 1 P. U. current, so the maximum allowed differential voltage (i.e., voltage across R69 - voltage between Y1 and Y2) is 10% of 20 volts or 2 volts. The differential voltage is applied to the series connection of the L2-R2 control winding and resistor R70. The resistance of R69 will be approximately

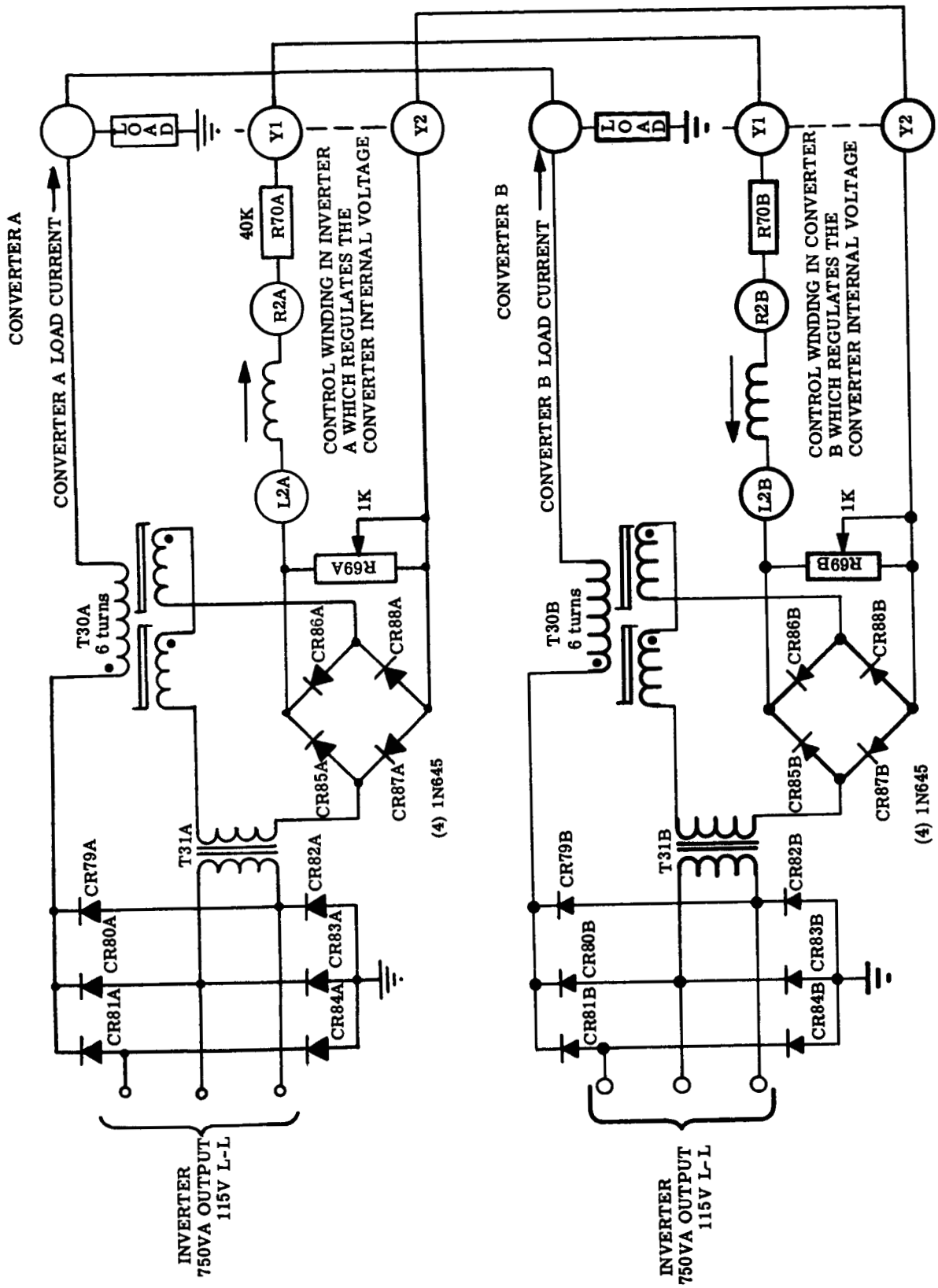


Figure 14. Schematic Diagram of the Converter Load Division Circuit

1K ohms and is very small compared to the resistance of R70. One milliampere of d-c current in the control winding will result in a 75 volt change in the internal voltage of the converter. This is a characteristic of the voltage regulator circuit used in the converter model and can be calculated or measured for any converter. The internal voltage is the voltage that would appear at the output terminals if the load were removed. The transfer curve for this d-c load division circuit would be very similar to that of Figure 11.

The gain of the differential current sensing circuit expressed as a function of R70 is as follows:

$$\frac{\partial E}{\partial I_{DR}} = \frac{-75 \text{ volts d-c}}{\text{ma. control current}} \times \frac{20 \text{ differential volts d-c}}{4.886 \text{ amps unbalanced current}}$$

$$\frac{\text{x } 1}{\text{R70}} \frac{\text{ma. control current}}{\text{differential volts d-c}} = \frac{-307}{\text{R70}} \frac{\text{volts d-c}}{\text{amps unbalanced current}}$$

where R70 is in K ohms.

Expressed in P. U. values: $\frac{\partial E}{\partial I_{DR}} = \frac{-307}{R70} \times \frac{4.886}{153.5} = \frac{9.78}{R70} \frac{\text{P. U. d-c volts}}{\text{P. U. d-c unbalanced current.}}$

The gain necessary to achieve load division unbalance no larger than 10% at full load is shown below.

The open loop gain of the regulator is expressed as follows:

$$\frac{\partial E}{\partial V_S} = \left| \frac{E_{F.L.} - V_{N.L.REG.}}{V_{N.L.REG.} - V_{F.L.REG.}} \right|$$

where $E_{F.L.}$ is the internal voltage necessary to obtain rated terminal voltage $V_{F.L.REG.}$ (at full load), and $E_{F.L.} = \left| \frac{\dot{Z}_1 + \dot{Z}_L}{\dot{Z}_L} \right| V_{F.L.REG.}$.

If the closed loop regulation is 0.7 volts line-to-neutral or .0061 P. U. volts and assuming $V_{N.L.REG.} = 1.0$ P. U. and $V_{F.L.REG.} = .9939$ P. U. volts, then

$$\frac{\partial E}{\partial V_S} = - \left| \frac{\left| \frac{\dot{Z}_1 + \dot{Z}_L}{\dot{Z}_L} \right| (.9939) - 1}{.0061} \right| ,$$

where $\dot{Z}_1 = .27 \angle 77.8°$ P.U. (Appendix IV), and $\dot{Z}_L$ must be determined: A resistive load on a three phase full wave bridge appears as an impedance of .955 power factor lagging (see Reference 2) to the source.

Also

$$I_{AC} = .816\, I_{DC}$$

The VA of the source is expressed as

$$VA = \sqrt{3}\, V_{AC\,LL}\, I_{AC}$$

so the watts supplied by the source, including the diode losses are:

$$W_T = \sqrt{3}\, V_{AC\,LL}\, I_{AC}\, (.955)$$

$$= \sqrt{3}\, (115)\, (.816)\, (4.886)(.955)$$

$$= 757.5 \text{ watts.}$$

Also

$$(I_{DC})^2\, R_L = 750 \text{ watts}$$

$$(I_{DC})^2\, R_{eq\,L} = 757.5 \text{ watts}$$

so $R_{eq\,L} = \frac{757.5}{750}\, R_L = 1.01$ P.U.

$$\therefore \dot{Z}_L = \frac{1.01}{.955} \angle \cos^{-1} .955 = 1.058 \angle \cos^{-1} .955 \text{ P.U.}$$

Knowing $\dot{Z}_1$ and $\dot{Z}_L$, the required voltage regulator gain can now be determined:

$$\frac{\partial E}{\partial V_S} = -\left| \frac{\left| .27 \angle 77.8 + 1.058 \angle \cos^{-1} .955 \right|}{\dfrac{1.058}{.0061}} (.9939) - 1 \right|$$

$$= -22.87$$

The gain of the converter voltage regulator will be set to this value.

Equation (33) of Appendix II is:

$$\Delta E = \left| E_{pL} - E_o \right| = (V_{pL} - V_{1L}) \frac{\partial E}{\partial V_s} + \frac{1}{K} (V_{1L} - V_o) + \frac{\partial E}{\partial I_{DR}} (\Delta I).$$

Assuming 115 ± .2 volts line-to-line voltage tolerance setting, then letting

$$V_{1L} = 1.00174 \text{ P.U.},$$

and $V_o = V_{pL} = 1.0$ P.U.

will give the maximum change.

So $\Delta E = .00174 (22.87 + 1.146) + \frac{\partial E}{\partial I_{DR}} (\Delta I)$

$$= .0419 + \frac{\partial E}{\partial I_{DR}} (\Delta I).$$

Since ΔI Max. = 0.1 P.U.

$$= \frac{\Delta E \text{ Max.}}{Z_1}$$

$$= \frac{\Delta E \text{ Max.}}{.27},$$

then ΔE Max. $= .027 = .0419 + \frac{\partial E}{\partial I_{DR}} (0.1).$

So $\frac{\partial E}{\partial I_{DR}} = \frac{.027 - .0419}{.1}$

$$= -.149 \frac{\text{P.U. a-c volts}}{\text{P.U. unbalance a-c current}}$$

$$= -\frac{.149}{.816} \frac{\text{P.U. a-c volts}}{\text{P.U. unbalanced d-c current}}$$

$$= -\frac{.149}{.816} \frac{(153.51)}{(115)} \frac{\text{P.U. d-c volts}}{\text{P.U. d-c unbalanced current}}$$

$$= -.244 \frac{\text{P.U. d-c volts}}{\text{P.U. d-c unbalanced current}}.$$

This is the required gain of the differential current sensing circuit.

Now R70 may be selected to give the required gain:

$$0.244 = \frac{9.78}{R70} ,$$

$$R70 = \frac{9.78}{0.244} = 40K \text{ ohms.}$$

VI. CONCLUSIONS

This report describes the requirements for successful paralleling of static inverters and converters. Circuits designed to meet these requirements are also described. A transformer design using field-annealed doubly oriented silicon steel is described with the expectation that its losses will be lower than an equivalent transformer using singly oriented silicon steel. Since all designs and concepts presented in this report will be experimentally evaluated during the remainder of this program, the conclusions drawn at this time must be hypothetical.

The use of Cubex steel as the core material for the quadratic transformer should result in a more efficient and/or lighter weight power transformer. Cubex steel has lower losses at high flux densities than do all other magnetic materials considered. Cubex steel also has two easy directions for magnetization compared with one for most other materials. The lower losses at high flux densities should improve the performance of all conventional transformers; i.e. toroidal, cut C cores, etc.). The property of two easy directions for magnetization is ideal for the type of output transformer core used in the inverter used in this study;(i.e., a core made up of planar laminations in which the flux must close its loop in the plane of the laminations).

Compared to a redundant inverter system, a parallel inverter system should be more reliable, have a higher power-to-weight ratio, and have more capacity for overloads.

The conditions for successfully paralleling static inverters/converters were determined and circuits were derived to meet those conditions.

The conditions necessary to parallel static inverters are that all inverters must operate at the same frequency, phase, nominal voltage, and they must have provisions to insure proper load division. The conditions necessary to parallel static converters are the same as those for inverters but the frequency is zero so it does not present a problem. The circuits that were derived to meet the above necessary conditions are described in the report.

The method used to parallel static inverters is to lock out all but one frequency reference and to connect that frequency reference to all inverters, then to lock all inverters in phase with one another and to sense differential load current of one phase and to change the internal voltage of each inverter such that the differential current tends to zero. The differential current sensing circuit is made most sensitive to the component of differential current that lags the

line-to-neutral terminal voltage by 60°. This particular method can be adapted to any type single or three-phase static inverters which can have their internal voltages locked in phase with the other inverters and which regulate the internal a-c voltage without affecting the phase relationship between paralleled inverters.

The method used to parallel static converters is to sense differential load current and to change the internal voltage of each converter such that the differential load current tends to zero. This method is applicable to any type regulated static converter.

APPENDIX I

The Effect of Incremental Changes in the Internal Voltage Source's Magnitude and Phase on the Phasor Components of the Differential Current in Parallel Voltage Source Systems

Consider the circuit of Figure 15 which represents a voltage source, E_1, with an internal impedance, Z_1, in parallel with similar units. There are in general two basic modes of steady state operation of this system of N paralleled units.

First Mode - Called equal load division. In this mode the total load ($\dot{I}_{Lp}$) is divided equally among the units. The subscript o will be used to identify quantities for this mode of operation, since the quantity would be equal for all units.

Second Mode - Called unequal load division. In this mode of operation the N units are assumed to be supplying the same total load at the same terminal voltage as in the first mode but now the load is assumed not to be divided equally among the units. The subscript 1 will be used to refer to unit number 1 quantities, subscript 2 for unit number 2 quantities and so forth.

A phasor diagram showing the quantities used in the following derivation is given in Figure 16.

For the first mode of operation, taking V_o as reference phasor, the equations for the various quantities become: *

(1) $\dot{V}_o = V_o \angle 0^o$; $v_o = \sqrt{2}\, V_o \sin(wt+o)$

(2) $\dot{I}_o = \dfrac{\dot{I}_{Lp}}{N} = \dfrac{1}{N}\dfrac{\dot{V}_o}{\dot{Z}_{Lp}} = \dfrac{V_o}{NZ_{Lp}} \angle -\Psi$

(3) $i_o = \dfrac{\sqrt{2}}{N}\dfrac{\dot{V}_o}{\dot{Z}_{Lp}} \sin(wt - \Psi)$, where Ψ is the total power factor angle.

The general node equation for Figure 15 is:

(4) $\dfrac{\dot{E}_1 - \dot{V}_t}{\dot{Z}_1} = \dot{I}_1$

*In all equations, small w is substituted for ω .

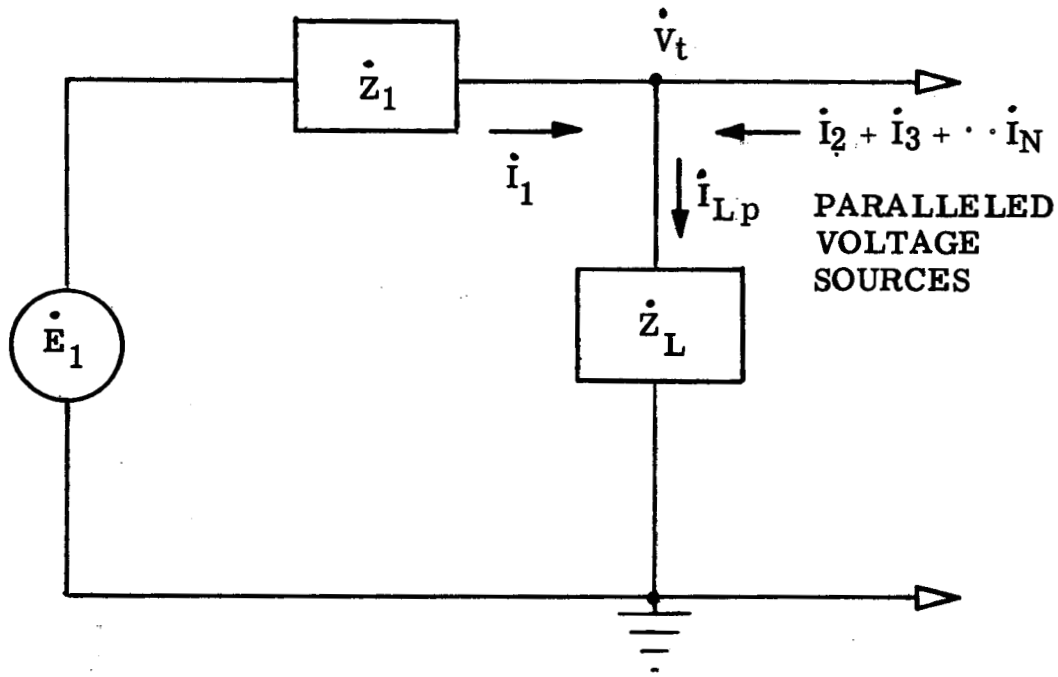


Figure 15. Equivalent Circuit of Voltage Source System

For the first mode type of operation,

$$\dot{I}_1 = \dot{I}_o;\ \dot{E}_1 = \dot{E}_o \text{ and } V_t = V_o \text{ therefore,}$$

$$(5)\quad \frac{\dot{E}_o - \dot{V}_o}{\dot{Z}_1} = \dot{I}_o;\ \dot{E}_o - \dot{V}_o = \dot{I}_o\dot{Z}_1.$$

Substitute Equation (3) into Equation (5):

$$(6)\quad e_o - v_o = \frac{\sqrt{2}}{\bar{N}} \frac{V_0 Z_1}{Z_{Lp}} \sin (wt - \Psi + \theta_1),$$

$$(7)\quad e_o = \frac{\sqrt{2}}{\bar{N}} \frac{V_o Z_1}{Z_{Lp}} \sin (wt - \Psi + \theta_1) + \sqrt{2}\ V_o \sin (wt), \text{ where } \theta \text{ is}$$

the phase angle of the internal impedance.

Using trig. formula for expansion of sine of sum of two angles:

$$(8)\quad e_o = \frac{\sqrt{2} V_o Z_1}{N\ Z_{Lp}} \cos\ (\theta_1 - \Psi) \sin wt + \frac{\sqrt{2}}{\bar{N}} \frac{V_o Z_1}{Z_{Lp}} \sin (\theta_1 - \Psi)$$

$$\times \cos wt + \sqrt{2}\ V_o \sin wt.$$

Collecting sin wt and cos wt terms:

$$(9)\quad e_o = \sqrt{2}\ V_o \left[\frac{Z_1}{NZ_{Lp}} \cos (\theta_1 - \Psi) + 1\right] \sin wt +$$

$$\sqrt{2}\ V_o \frac{Z_1}{NZ_{I\cdot p}} \sin (\theta_1 - \Psi) \cos wt.$$

But

$$(10)\quad e_o = \sqrt{2}\ E_o \sin (wt + \theta_o), \text{ where } \theta_o \text{ is the angle between the internal}$$

voltage, E_o, and the terminal voltage, V_o.

Or

$$(11)\quad e_o = \sqrt{2}\ E_o \cos \theta_o \sin wt + \sqrt{2}\ E_o \sin \theta_o \cos wt.$$

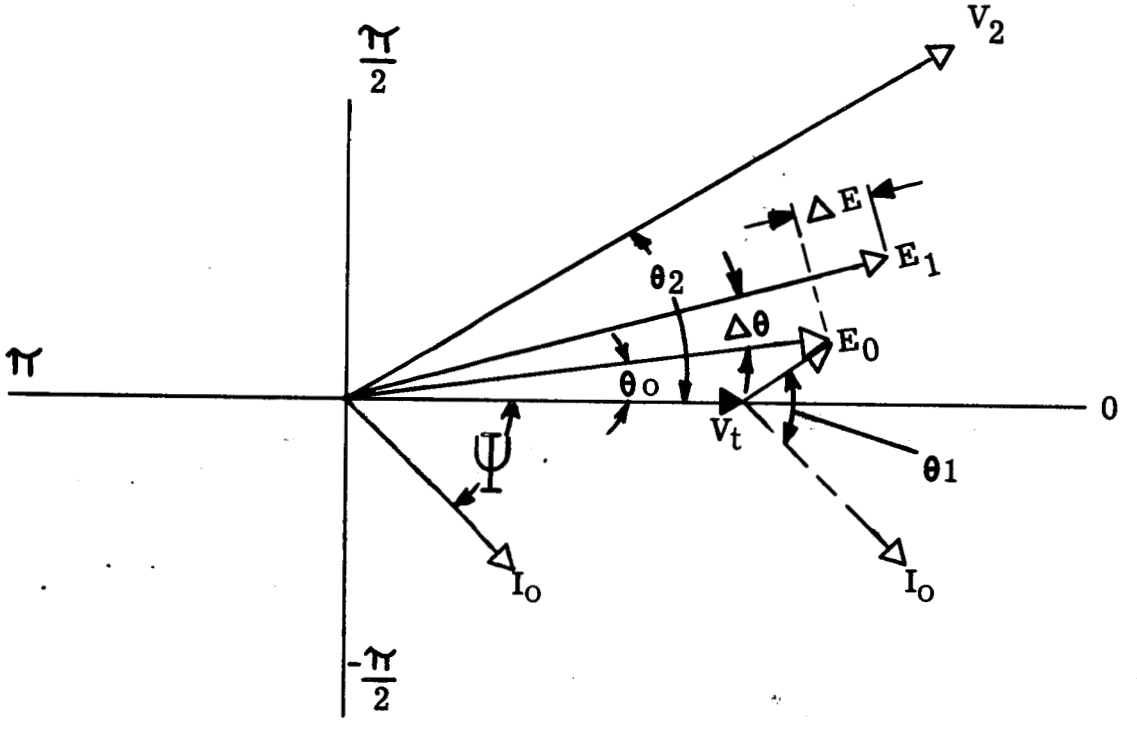


Figure 16. Phasor Diagram Showing Quantities and Parameters Used in Appendix I Derivation

Comparing Equations (9) and (11), the following results:

$$(12)\quad \sqrt{2}\, E_o \cos\theta_o = \sqrt{2}\, V_o \left[\frac{Z_1}{NZ_{Lp}} \cos(\theta_1 - \Psi) + 1\right],$$

$$(13)\quad \sqrt{2}\, E_o \sin\theta_o = \sqrt{2}\, V_o \frac{Z_1}{NZ_{Lp}} \sin(\theta_1 - \Psi).$$

Therefore,

$$(14)\quad \tan\theta_0 = \frac{\frac{Z_1}{NZ_{Lp}} \sin(\theta_1 - \Psi)}{1 + \frac{Z_1}{NZ_{Lp}} \cos(\theta_1 - \Psi)}.$$

For the second mode type of operation, let $\dot{E}_1$ differ from $\dot{E}_o$ in the following manner:

$$(15)\quad e_1 = \sqrt{2}\,(E_o + \Delta E) \sin(wt + \theta_o + \Delta\theta).$$

Let us require $\dot{V}_t$ for the unbalanced condition be the same as $\dot{V}_o$ and substract Equation (5) from Equation (4):

$$(16)\quad \dot{I}_1 - \dot{I}_o = \frac{\dot{E}_1 - \dot{E}_o}{\dot{Z}_1},$$

$$(17)\quad (i_1 - i_o) = \frac{\sqrt{2}\,(E_o + \Delta E)}{Z_1} \sin(wt + \theta_o + \Delta\theta - \theta_1) - \frac{\sqrt{2}\,E_o}{Z_1} \sin(wt + \theta_o - \theta_1)$$

Expanding the sine of the sum of two angles:

$$(18)\quad (i_1 - i_o) = \frac{\sqrt{2}\,(E_o + \Delta E)}{Z_1} \cos\Delta\theta \sin(wt + \theta_o - \theta_1) - \frac{\sqrt{2}\,E_o}{Z_1} \times \sin(wt + \theta_o - \theta_1) + \frac{\sqrt{2}\,(E_o + \Delta E)}{Z_1} \sin\Delta\theta \cos(wt + \theta_o - \theta_1).$$

Combining terms and then expanding $\sin(wt + \theta_o - \theta_1)$ and $\cos(wt + \theta_o - \theta_1)$:

$$(19)\quad (i_1 - i_o) = \left[\frac{\sqrt{2}(E_o + E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right]\cos(\theta_o - \theta_1)\sin wt$$
$$+\left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right]\sin(\theta_o - \theta_1)\cos wt$$
$$+\left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\sin\Delta\theta\right]\cos(\theta_o - \theta_1)\cos wt$$
$$-\left[\frac{\sqrt{2}(E_o + \Delta E_o)}{Z_1}\sin\Delta\theta\right]\sin(\theta_o - \theta_1)\sin wt.$$

Collecting sin (wt) and cos (wt) terms

$$(20)\quad (i_1 - i_o) = \left[\left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right)\cos(\theta_o - \theta_1)\right.$$
$$\left. - \frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\sin\Delta\theta\sin(\theta_o - \theta_1)\right]\sin wt$$
$$+\left[\left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right)\sin(\theta_o - \theta_1)\right.$$
$$\left. + \frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\sin\Delta\theta\cos(\theta_o - \theta_1)\right]\cos wt.$$

Since the terminal (Bus) voltage was taken as the reference, the coefficient of the sin (wt) term in Equation (20) will be the real component of $(i_1 - i_o)$ (component in phase with bus voltage) and the coefficient of the cos (wt) term in Equation (20) will be the reactive component of $(i - i_a)$ (component at right angles to bus voltages).

Therefore:

$$(21)\quad R(\dot{I}_1 - \dot{I}_o) = \left(\frac{(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{E_o}{Z_1}\right)\cos(\theta_o - \theta_1)$$
$$-\frac{(E_o + \Delta E)}{Z_1}\sin\Delta\theta\sin(\theta_o - \theta_1).$$

$$(22)\quad Q(\dot{I}_1 - I_o) = \left(\frac{(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{E_o}{Z_1}\right)\sin(\theta_o - \theta_1)$$

$$+ \left(\frac{E_o + \Delta E}{Z_1}\right)\sin\Delta\theta\cos(\theta_o - \theta_1).$$

If $\Delta\theta$ and ΔE are very small:

$\cos\Delta\theta = 1$; $\sin\Delta\theta = \Delta\theta$ radians; $(E_o + \Delta E) \cong E_o$.

Then Equations (21) and (22) become:

$$(23)\quad R(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1}\cos(\theta_o - \theta_1) - \frac{E\Delta\theta}{Z_1}\sin(\theta_o - \theta_1)\quad,$$

$$(24)\quad Q(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1}\sin(\theta_o - \theta_1) + \frac{E_o\Delta\theta}{Z_1}\cos(\theta_o - \theta_1).$$

It is desirable to have equations of the components of $(\dot{I}_1 - \dot{I}_o)$ with respect to a phasor other than the terminal voltage of the phase in which current is being sensed. Therefore, consider Equation (18) once more. It could be written as follows, where θ_2 is any angle:

$$(18a)\quad (i_1 - i_o) = \frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta\sin\left[wt + \theta_2 + (\theta_o - \theta_1 - \theta_2)\right]$$

$$- \frac{\sqrt{2}E_o}{Z_1}\sin\left[wt + \theta_2 + (\theta_o - \theta_1 - \theta_2)\right]$$

$$+ \frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\sin\Delta\theta\cos\left[wt + \theta_2 + (\theta_o - \theta_1 - \theta_2)\right].$$

Combining terms and then expanding $\sin\left[wt + \theta_2 + (\theta_o - \theta_1 - \theta_2)\right]$ and $\cos\left[wt + \theta_2 + (\theta_o - \theta_1 - \theta_2)\right]$:

$$(19a)\quad (i_1 - i_o) = \left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right]\cos(\theta_o - \theta_1 - \theta_2)$$

$$\times \sin(wt + \theta_2)$$

$$+\left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right]\sin(\theta_o - \theta_1 - \theta_2)\cos(wt + \theta_2)$$

$$+ \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \cos(\theta_o - \theta_1 - \theta_2) \cos(wt + \theta_2)$$

$$- \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \sin(\theta_o - \theta_1 - \theta_2) \sin(wt + \theta_2) .$$

Collecting $\sin(wt+\theta_2)$ and $\cos(wt+\theta_2)$ terms:

$$(20a) \quad (i_1 - i_o) = \left[\left(\frac{\sqrt{2}(E_o + \Delta E_o)}{Z_1} \cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right) \cos(\theta_o - \theta_1 - \theta_2)\right.$$

$$\left. - \left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin\Delta\theta\right) \sin(\theta_o - \theta_1 - \theta_2)\right] \sin(wt + \theta_2)$$

$$+ \left[\left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right) \sin(\theta_o - \theta_1 \theta_2)\right.$$

$$\left. + \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin\Delta\theta \cos(\theta_o - \theta_1 - \theta_2)\right] \cos(wt + \theta_2) .$$

Since the terminal voltage (line-to-neutral voltage of the phase in which differential current is measured) was taken as reference, the coefficient of the $\sin(wt+\theta_2)$ term in Equation (20a) is the component of $(i-i_o)$ in phase with a phasor θ_2 degrees ahead of the terminal voltage and the coefficient of the $\cos(wt+\theta_2)$ term in Equation (20a) is the component of $(i-i_o)$ at right angles with a phasor θ_2 degrees ahead of the terminal voltage.

Therefore:

$$(23d) \quad R_{\theta_2}(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1} \cos(\theta_o - \theta_1 - \theta_2) - \frac{E\Delta\theta}{Z_1} \sin(\theta_o - \theta_1 - \theta_2),$$

$$(24d) \quad Q_{\theta_2}(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1} \sin(\theta_o - \theta_1 - \theta_2) + \frac{E\Delta\theta}{Z_1} \cos(\theta_o - \theta_1 - \theta_2) .$$

APPENDIX II

The Effect of Voltage Regulator Adjustments on the Steady-State Unbalance of Load Currents in a System of Parallel Connected Voltage Sources

Consider an inverter (or alternator or other voltage source) that is operating "open loop". That is, the voltage regulator sensing circuit is not connected to the output bus. It is connected to a separate voltage source, V_S. In a like manner, the "reactive" load division current transformer (or any other sensing device that might be used) is operated "open loop" and is connected to a separate supply.

With the voltage applied to the voltage regulator sensing circuit (V_S) equal to V_0 volts, let the regulator setting be such that the terminal voltage (V_t) is also equal to V_0 volts. (A load of Z_L ohms assumed connected to the output.) Let us denote this regulator setting as R_{SO} and the resulting value of the internal voltage as E_0. (No signal applied to "reactive" load division circuit.)

Any change in V_S from V_0 will now result in E changing from the value of E_0. Any change in the R_S setting from R_{SO} will also result in E changing from E_0. Also, if a signal is applied to the "reactive" load circuit, E will change from E_0. If all these changes occur at the same time, the net change in E will be equal to the algebraic sum of the changes due to each cause acting independently. If we denote the quantity $(E-E_0)$ as ΔE, the quantity (V_S-V_0) as ΔV_S, the quantity (R_S-R_{SO}) as ΔR_S, and the differential "quadrature" component of current as ΔI_Q, we can express this mathematically as:

$$(25) \quad \Delta E = \frac{\partial E}{\partial V_S} \Delta V_S + \frac{\partial E}{\partial R_S} \Delta R_S + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q .$$

The quantities $\frac{\partial E}{\partial V_S}$, $\frac{\partial E}{\partial R_S}$, $\frac{\partial E}{\partial I_{DQ}}$ denote the corresponding control circuit "open loop" gain. How these gains are achieved; that is, what circuitry is used, is of no concern in the development of the relationship that follows. These relationships are of a general nature and hold for a variety of regulating methods.

For closed loop operation ($V_S = V_t$) of a loaded single unit system and regulator setting R_S different from R_{SO}, Equation (25) becomes:

$$(26) \quad (E_{1L}-E_0) = \frac{\partial E}{\partial V_S} (V_{1L}-V_0) + \frac{\partial E}{\partial R_S} (R_S-R_{SO}) ;$$

where E_{1L} and V_{1L} denote the value of the quantities E and $V_t = V_s$, for regulator as set and operating as a single unit system.

But for a fixed load on a single unit system the following is a general relationship:

$$(27) \quad V_t = \left[\frac{Z_L}{|\bar{Z}_1+\bar{Z}_L|}\right] E_1 = KE_1$$

where V_t is the terminal voltage and E_1 is the internal voltage for any particular set of conditions. Therefore $V_o = KE_o$ and $V_{1L} = KE_{1L}$ and

$$(28) \quad V_{1L}-V_o = KE_{1L} - KE_o = K\left[E_{1L} - E_o\right],$$

and Equation (26) becomes:

$$(29) \quad (E_{1L} - E_o)\left[1 - K\frac{\partial E}{\partial V_s}\right] = \frac{\partial E}{\partial R_s}(R_s - R_{so}).$$

Now let us further require that the V_o, E_o, and R_{so} values of V_s, E, and R_s used above be the necessary values of V_s, E, and R_s for the unit to operate in a parallel system with zero differential current.

For parallel operation under closed loop control $V_s = V_{pL}$ ≡ bus voltage of loaded parallel system and Equation (25) becomes:

$$(30) \quad (E_{pL} - E_o) = \frac{\partial E}{\partial V_s}(V_{pL} - V_o) + \frac{\partial E}{\partial R_s}(R_s - R_{so}) + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q$$

Substituting Equation (29) into (30) we have:

$$(31) \quad (E_{pL} - E_o) = \frac{\partial E}{\partial V_s}(V_{pL} - V_o) + (E_{1L} - E_o)\left[1 - K\frac{\partial E}{\partial V_s}\right] + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q$$

or

$$(32) \quad (E_{pL} - E_o) = (V_{pL} - V_o - KE_{1L} + KE_o)\frac{\partial E}{\partial V_s} + (E_{1L} - E_o) + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q$$

or

$$(33) \quad (E_{pL} - E_o) = (V_{pL} - V_{1L})\frac{\partial E}{\partial V_s} + \frac{1}{K}(V_{1L} - V_o) + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q.$$

If the bus voltage of the loaded parallel system is the same for Mode One type operation (equal load division) as for the Mode Two type operation

(unequal load division), $V_{pL} = V_o$, we could then express Equation (33) as

$$(33a)\quad \Delta E = (E_{pL} - E_o) = \left[\frac{1}{K} - 1\right](V_{1L} - V_{pL})\frac{\partial E}{\partial V_s} + \frac{\partial E}{\partial I_{DQ}}\Delta I_Q .$$

Equation (33) and/or (33a) relate single-unit operation to parallel-system operation. The voltage regulator circuit gain, $\frac{\partial E}{\partial V_s}$, is a function of the single-unit-operation voltage regulation requirements. If the internal impedance is known the necessary value of $\frac{\partial E}{\partial V_s}$ can be calculated from the voltage regulation specifications. V_{1L} depends on how close each unit (operating independently as a single unit system) can be expected to regulate to the same voltage. In fact if all units regulated to exactly the same voltage under all loading conditions, there would be no need for a load division circuit when the units are operated in parallel. The value of V_{1L} to be used in Equation (33) and/or (33a) is taken equal to the regulated voltage of the unit that, for any allowable reason, regulates farthest from nominal voltage of the specification for V_{pL}.

In Appendix I, Equation (24d) relates ΔE, ΔI_Q, and Z_1. If the maximum allowable value of ΔI_Q is specified and Z_1 is known, the required value of $\frac{\partial E}{\partial I_{DQ}}$ can be calculated using Equation (24d) and Equation (33a). A method for calculating Z_1 is given in Appendix III. An example of the calculations suggested above is given in Appendix IV.

APPENDIX III

Method of Calculating Balanced Load Internal Impedance of a Four-Power-Stage Three-Phase Static Inverter

When first presented, the problem of determining analytically the internal impedance of a static inverter which used a harmonic interchange transformer connection appeared to require the solution of a very large number of long simultaneous equations if any degree of rigor were to be required.

It was felt that a digital computer program would be required to aid in the investigation of the relative importance of various parameters as to internal impedance. It was hoped that, as insight into the problem was then gained, a slightly less complicated method of calculation could be developed lending itself to hand calculations.

As there was a definite time limit involved, it was felt this could best be done using a modification of a digital computer program already in existence for an inverter other than the subject NASA inverter. Many of the needed constants were already available for this other inverter. Actual test information was also available for this inverter. There was even the possibility of experimentally checking some of the analytical results that one would obtain. All of these considerations pointed to using a study of this other inverter to gain insight into the problem rather than starting from scratch and developing a computer program, constants, etc., for a different inverter. This plan was followed.

As insight and experience were gained on the "internal impedance" problem, a method was devised to calculate the "balanced condition" internal impedance without the aid of a digital computer. The development of this method is presented in this appendix.

The schematic diagram of the particular output transformer which will be used in the test model inverters in given in Figure 17. The equation derived in this section gives the impedance looking into the terminals of Phase 1. Equation (75) can be applied to inverters with any number of power stages, although the derivation is based on a four-power-stage inverter. The following assumptions and definitions are an essential part of this derivation.

1. Let the subscript p refer to 1/2 the primary winding of any power stage (all power stages' primary windings assumed the same).

2. Let all the secondary windings of the power stages in Phase 1 be designated winding #1 for that stage.

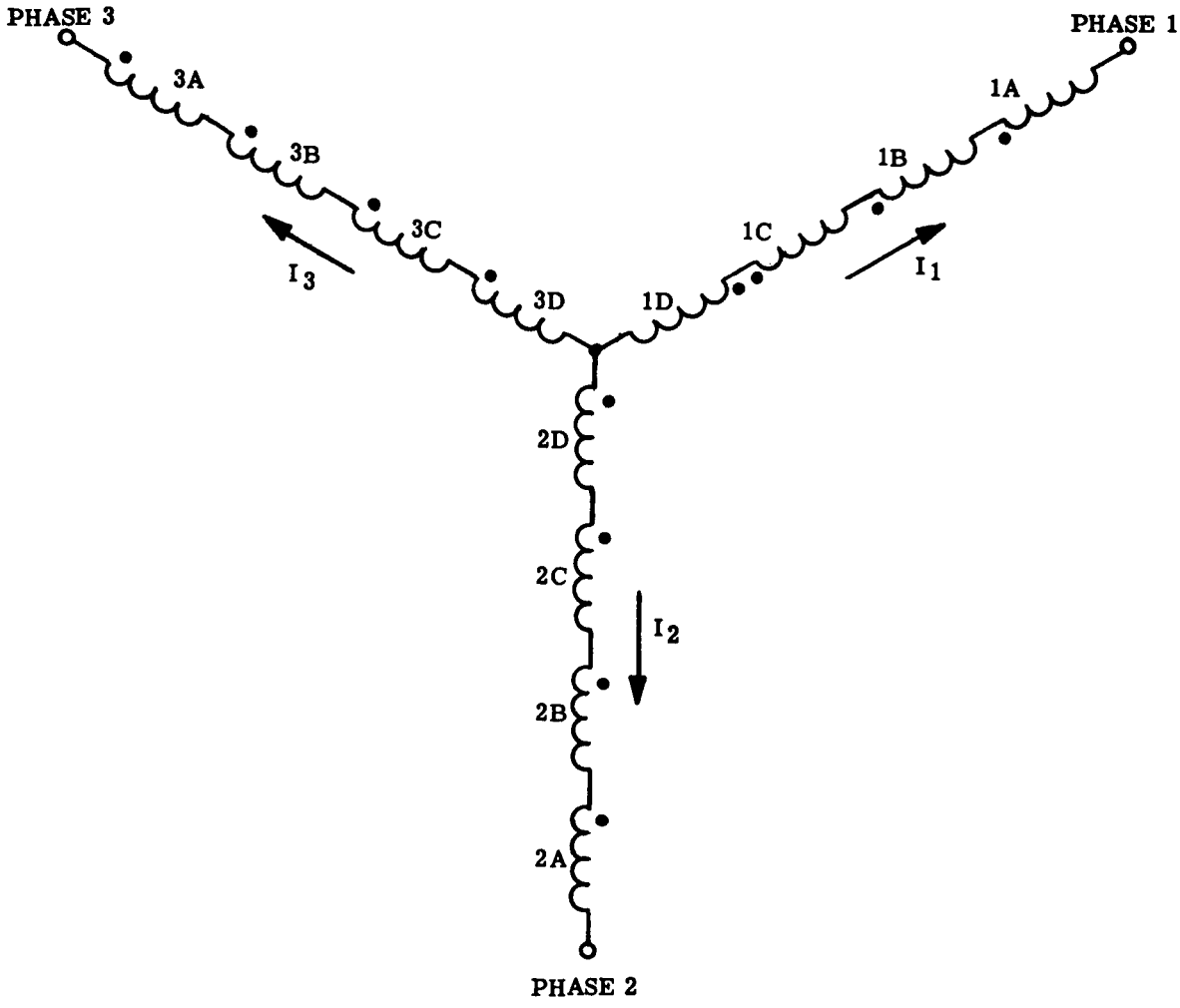


Figure 17. Schematic Diagram of Output Transformer Secondary Connections

3. Let all the secondary windings of the power stages that are in Phase 2 be designated winding #2 for that stage.

4. Let all the secondary windings of the power stages that are in Phase 3 be designated winding #3 for that stage.

5. Let all number of turns of a winding be expressed in P.U., based on 1/2 the primary winding of power stage as base value.

6. Let L_{pp}, L_{11}, L_{22}, etc., be defined in the following manner. The voltage drop $jwI_p(L_{pp})$ is the voltage induced in winding p by that part of the flux, due to I_p, which lies entirely or partially outside the iron core (core-self-leakage inductance of winding p). In the work that follows, assume that all constants and voltages are referred to 1/2 the primary winding and expressed in inverter per unit (P.U.). The secondary currents (phase currents I_1, I_2, I_3 are in P.U. not referred to primary).

7. Let L_{p1}, L_{12}, L_{23}, etc. be defined in the following manner. The quantity $w(L_{p1})$ is the core-mutual-leakage reactance of winding p with respect to winding 1 or of winding 1 with respect to winding p. It differs from the mutual reactance between winding p and 1 by being caused by only that portion of the mutual flux, of those two windings, that does not lie entirely within the core.

8. Define a true leakage reactance of winding p with respect to winding 1 ($wL_{p(1)}$) as follows. This true leakage reactance of one winding with respect to another is the reactance used in the treatment of the conventional two-winding transformer. The true leakage reactance of winding p with respect to winding 1 is caused by that part of the flux, due to I_p, which does not link winding 1. It may produce linkage with windings 2 or 3 or with other windings if there are more than four. Thus,

$$w\ L_{p(1)} = wL_{pp} - wL_{p1}.$$

Refer to Figure 18. This sketch may help to clarify the definitions (6, 7, and 8) pertaining to leakage reactances. The sketch shows some typical leakage flux paths in a three winding transformer when only the primary winding, p, conducts current. Solid line flux links winding p only. Long dash-short dash line flux links winding p and winding 1. Dashed line flux links all three windings.

The flux that is associated with the core-self-leakage reactance L_{pp} would be the sum of the three types of leakage flux illustrated. (Solid line + [long dash-short dash line] + short dash line.)

The flux that is associated with the core-mutual-leakage reactance of winding p with respect to winding 1, L_{p1}, would be the sum of the fluxes illustrated by the long dash-short dash lines and the short dash lines.

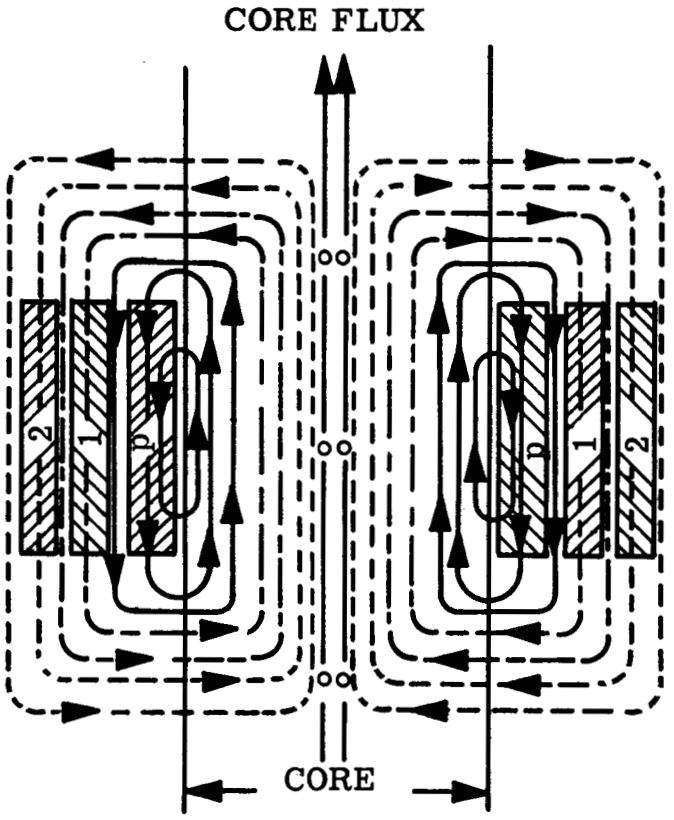


Figure 18. Flux Due to Current in Winding p of a Three Winding Transformer

The flux associated with the core-mutual-leakage reactance of winding p with respect to winding 2, L_{p2}, would be illustrated by the short dash lines only.

The flux associated with the true leakage reactance of winding p with respect to winding 1, $L_{p(1)}$, would be illustrated by the solid lines only.

The flux associated with the true leakage reactance of winding p with respect to winding 2, $L_{p(2)}$, would be the sum of the fluxes illustrated by solid lines and the long dash-short dash lines.

9. Define the sum $\sum_{S21} (N_2)\ (N_1)\ (wL_{2(p)} - wL_{2(1)})$ as the arithemtic sum of the leakage reactances for all power stages that have secondary windings in both Phase 2 and Phase 1. The sign of the term to be considered positive if the assumed directions for the phase currents both enter the dot terminals or both leave the dot terminals of the particular secondary windings. In the work to follow, all three phase currents are assumed to flow out from neutral point when they are positive.

   NOTE: N's are in P.U. and L's are referred to p and are in P.U.

10. Define the sum $\sum_{S31} (N_3)\ (N_1)\ (wL_{3(p)} - wL_{3(1)})$ similar to 9 above except for all power stages that have secondary windings in both Phase 3 and Phase 1.

11. Define the sum $\sum_{S1} (N_1)^2\ (R_{11} + jwL_{1(p)})$ as the sum of the impedances of all the secondary windings connected in series in Phase 1. All terms are taken to be positive.

12. T.R. - transformer ratio. This is the ratio of transformer open circuit secondary Phase 1 voltage to the fundamental RMS primary applied voltage of the power stage assumed to be excited first. Therefore, it is a phasor quantity. It can be calculated as:

$$\dot{T.R.} = \sum_{S1} \dot{N}_1 = |\dot{T.R.}|\ \angle\theta_R,$$

where the number of turns, N, (in P.U.) are considered phasors. The phasor angle 0° is assigned to that stage whose primary is assumed to be excited positive first. Each succeeding stage (in order of excitation) has its assigned phasor angle $\frac{180°}{NS}$ less than previous excited stage.

NS = total number of power stages. The sign before a term is taken

positive if the assumed Phase 1 current flows out of the dot terminal of the corresponding secondary winding. Refer to Figure 19 for a phasor plot for phase one of the transformer connections shown in Figure 17.

13. Define the sum $\sum_{S1} (\dot{N}_1)\,(R_p + jwL_{p(1)})$ as the phasor sum of the products of primary impedance times P.U. phasor turns of the winding of that stage in Phase 1. The angles assigned to the turns and the sign before each term is the same as in 12 preceding.

Four fundamental equations can be written for each of the power stage transformers, shown in Figures 20 - 23, in terms of core-self-leakage inductance and core-mutual-leakage inductance, as follows:

(36) $\dot{E}_{pA} = \dot{I}_{pA}\,(R_{pA} + jwL_{ppA}) + \dot{I}_1\,(N_{1A})\,jwL_{1pA} - \dot{I}_2\,(N_{2A})\,jwL_{2pA} - \dot{I}_3\,(N_{3A})jwL_{3pA} + \dot{E}_{CA}$

(37) $\dot{E}_{1A} = \dot{I}_{pA}jwL_{p1A} + \dot{I}_1\,(N_{1A})(R_{11A} + jwL_{11A}) - \dot{I}_2(N_{2A})\,jwL_{21A} - \dot{I}_3\,(N_{3A})\,jwL_{31A} + \dot{E}_{CA}$

(38) $\dot{E}_{2A} = \dot{I}_{pA}jwL_{p2A} + \dot{I}_1\,(N_{1A})\,jwL_{12A} - \dot{I}_2\,(N_{2A})(R_{22A} + jwL_{22A}) - \dot{I}_3\,(N_{3A})jwL_{32A} + \dot{E}_{CA}$

(39) $\dot{E}_{3A} = \dot{I}_{pA}jwL_{p3A} + \dot{I}_1(N_{1A})jwL_{13A} - \dot{I}_2(N_{2A})jwL_{23A} - \dot{I}_3(N_{3A})(R_{33A} + jwL_{33A}) + \dot{E}_{CA}$

(40) $\dot{E}_{pB} = \dot{I}_{pB}(R_{pB} + jwL_{ppB}) + \dot{I}_1(N_{1B})jwL_{1pB} - \dot{I}_2(N_{2B})jwL_{2pB} - \dot{I}_3\,(N_{3B})jwL_{3pB} + \dot{E}_{CB}$

(41) $\dot{E}_{1B} = \dot{I}_{pB}jwL_{p1B} + \dot{I}_1(N_{1B})(R_{11B} + jwL_{11B}) - \dot{I}_2(N_{2B})jwL_{21B} - \dot{I}_3(N_{3B})jwL_{31B} + \dot{E}_{CB}$

(42) $\dot{E}_{2B} = \dot{I}_{pB}jwL_{p2B} + \dot{I}_1(N_{1B})jwL_{12B} - \dot{I}_2(N_{2B})(R_{22B} + jwL_{22B}) - \dot{I}_3(N_{3B})jwL_{32B} + \dot{E}_{CB}$

(43) $\dot{E}_{3B} = \dot{I}_{pB}jwL_{p3B} + \dot{I}_1(N_{1B})jwL_{13B} - \dot{I}_2(N_{2B})jwL_{23B} - \dot{I}_3(N_{3B})(R_{33B} + jwL_{33B}) + \dot{E}_{CB}$

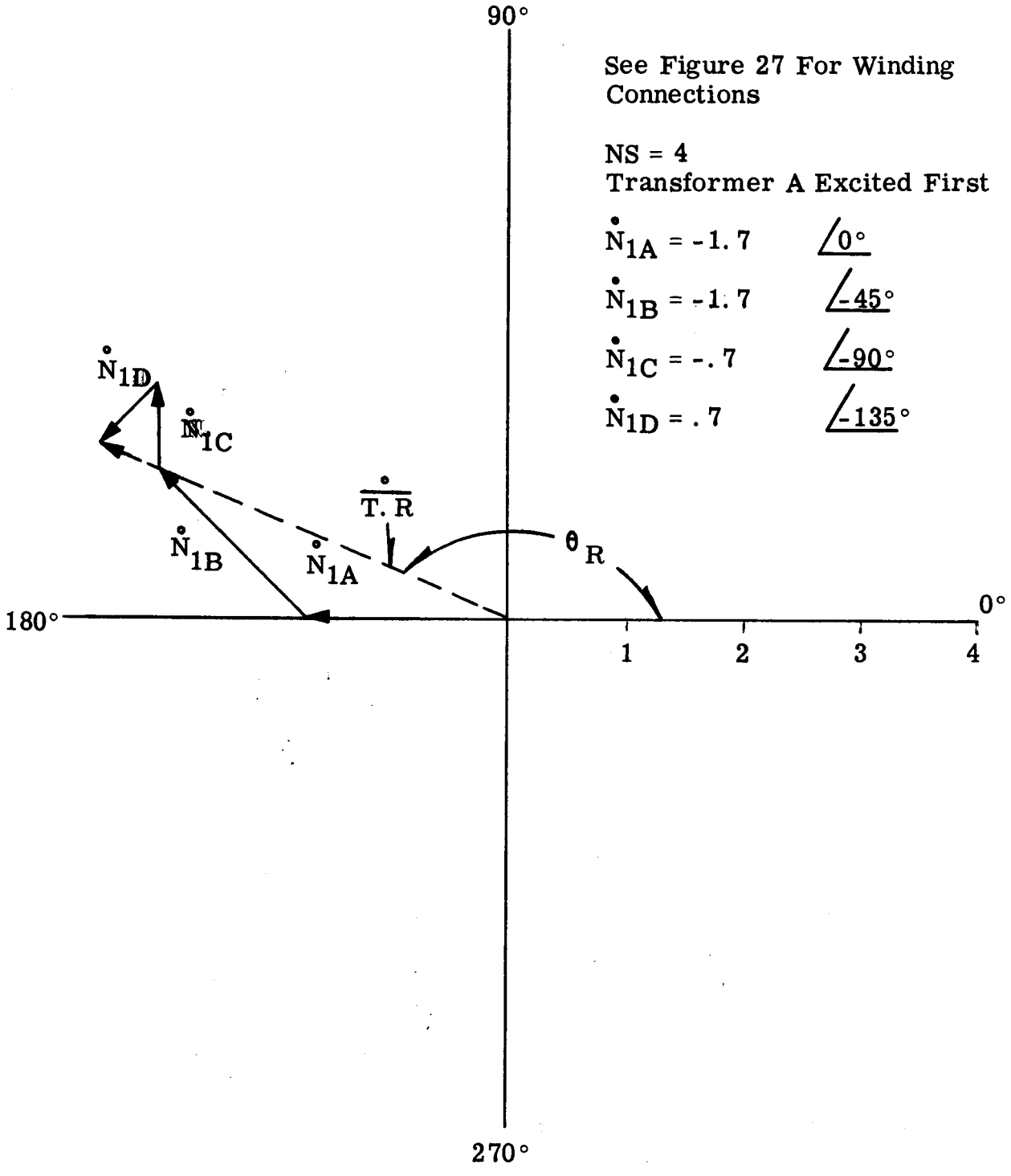


Figure 19. Phasor Diagram for Phase One $\overline{\dot{T}.R}$.

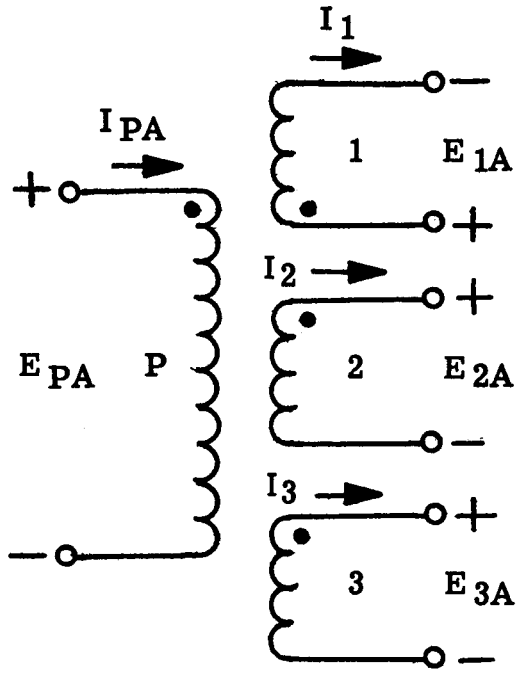


Figure 20. Schematic Diagram of Transformer Winding on Leg A

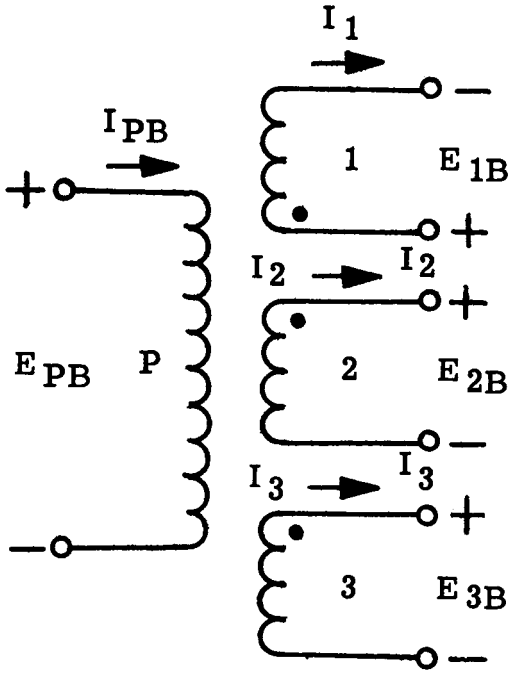


Figure 21. Schematic Diagram of Transformer Winding on Leg B

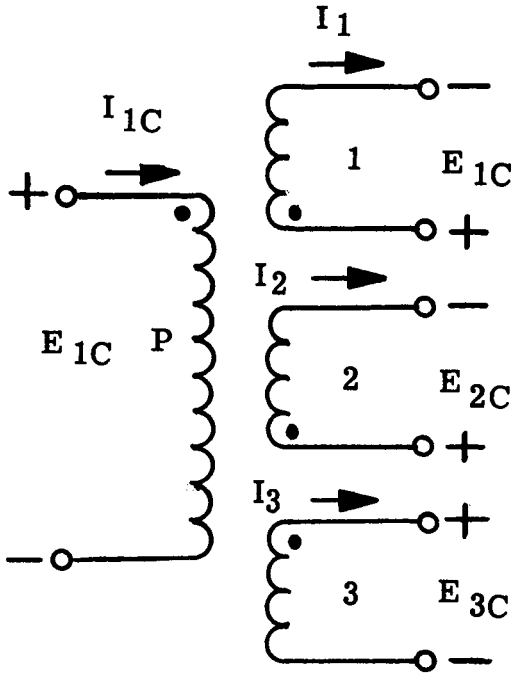


Figure 22. Schematic Diagram of Transformer Winding on Leg C

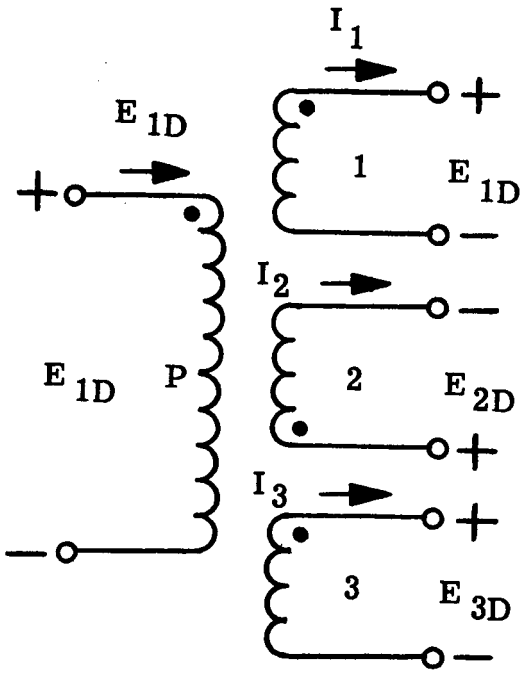


Figure 23. Schematic Diagram of Transformer Winding on Leg D

$$(44)\quad \dot{E}_{pC} = \dot{I}_{pC}(R_{pC} + jwL_{ppC}) + \dot{I}_1(N_{1C})jwL_{1pC} + \dot{I}_2(N_{2C})jwL_{2pC} - \dot{I}_3(N_{3C})jwL_{3pC} + \dot{E}_{CC}$$

$$(45)\quad \dot{E}_{1C} = \dot{I}_{pC}jwL_{p1C} + \dot{I}_1(N_{1C})(R_{11C} + jwL_{11C}) + \dot{I}_2(N_{2C})jwL_{21C} - \dot{I}_3(N_{3C})jwL_{31C} + \dot{E}_{CC}$$

$$(46)\quad \dot{E}_{2C} = \dot{I}_{pC}jwL_{p2C} + \dot{I}_1(N_{1C})jwL_{12C} + \dot{I}_2(N_{2C})(R_{22C} + jwL_{22C}) - \dot{I}_3(N_{3C})jwL_{32C} + \dot{E}_{CC}$$

$$(47)\quad \dot{E}_{3C} = \dot{I}_{pC}jwL_{p3C} + \dot{I}_1(N_{1C})jwL_{13C} + \dot{I}_2(N_{2C})jwL_{23C} - \dot{I}_3(N_{3C})(R_{33C} + jwL_{33C}) + \dot{E}_{CC}$$

$$(48)\quad \dot{E}_{pD} = \dot{I}_{pD}(R_{pD} + jwL_{ppD}) - \dot{I}_1(N_{1D})jwL_{1pD} + \dot{I}_2(N_{2D})jwL_{2pD} - \dot{I}_3(N_{3D})jwL_{3pD} + \dot{E}_{CD}$$

$$(49)\quad \dot{E}_{1D} = \dot{I}_{pD}jwL_{p1D} - \dot{I}_1(N_{1D})(R_{11D} + jwL_{11D}) + \dot{I}_2(N_{2D})jwL_{21D} - \dot{I}_3(N_{3D})jwL_{31D} + \dot{E}_{CD}$$

$$(50)\quad \dot{E}_{2D} = \dot{I}_{pD}jwL_{p2D} - \dot{I}_1(N_{1D})jwL_{12D} + \dot{I}_2(N_{2D})(R_{22D} + jwL_{22D}) - \dot{I}_3(N_{3D})jwL_{32D} + \dot{E}_{CD}$$

$$(51)\quad \dot{E}_{3D} = \dot{I}_{pD}jwL_{p3D} - \dot{I}_1(N_{1D})jwL_{13D} + \dot{I}_2(N_{2D})jwL_{23D} - \dot{I}_3(N_{3D})(R_{33D} + jwL_{33D}) + \dot{E}_{CD}$$

The line-to-neutral voltage of phase 1 in Figure 17 is:

$$(52)\quad \dot{E}_{LN1} = (N_{1A})\dot{E}_{1A} - (N_{1B})\dot{E}_{1B} - (N_{1C})\dot{E}_{1C} + (N_{1D})\dot{E}_{1D}$$

However,

$$(53)\quad \dot{E}_{pA} - \dot{E}_{1A} = \text{Eq. (36) - Eq. (37)}$$
$$= \dot{I}_{pA}\left[R_{pA} + jw(L_{ppA} - L_{p1A})\right] - \dot{I}_1(N_{1A})\left[R_{11A} + jw(L_{11A} - L_{1pA})\right] - \dot{I}_2(N_{2A})jw(L_{2pA} - L_{21A}) - \dot{I}_3(N_{3A})jw(L_{3pA} - L_{31A})$$

or since

$$(54)\quad (L_{2pA}-L_{21A}) = (L_{22A}-L_{21A}) - (L_{22A}-L_{2pA}) = L_{2(1)A} - L_{2(p)A}$$

$$(55)\quad (L_{3pA}-L_{31A}) = (L_{33A}-L_{31A}) - (L_{33A}-L_{3pA}) = L_{3(1)A} - L_{3(p)A}$$

$$(56)\quad \dot{E}_{pA}-\dot{E}_{1A} = \dot{I}_{pA}(R_{pA}+jwL_{p(1)A}) - \dot{I}_1(N_{1A})(R_{11A}+jwL_{1(p)A}) - \dot{I}_2(N_{2A})jw(L_{2(1)A} - L_{2(p)A}) - \dot{I}_3(N_{3A})jw(L_{3(1)A} - L_{3(p)A})$$

In a similar manner the following equations result.

$$(57)\quad \dot{E}_{pB}-\dot{E}_{1B} = \dot{I}_{pB}(R_{pB}+jwL_{p(1)B}) - \dot{I}_1(N_{1B})(R_{11B}+jL_{1(p)B}) - \dot{I}_2(N_{2B})jw(L_{2(1)B}-L_{2(p)B}) - \dot{I}_3(N_{3B})jw(L_{3(1)B}-L_{3(p)B})$$

$$(58)\quad \dot{E}_{pC}-\dot{E}_{1C} = \dot{I}_{pC}(R_{pC}+jwL_{p(1)C}) - \dot{I}_1(N_{1C})(R_{11C}+jwL_{1(p)C}) + \dot{I}_2(N_{2C})jw(L_{2(1)C}-L_{2(p)C}) - \dot{I}_3(N_{3C})jw(L_{3(1)C}-L_{3(p)C})$$

$$(59)\quad \dot{E}_{pD}-\dot{E}_{1D} = \dot{I}_{pD}(R_{pD}+jwL_{p(1)D}) + \dot{I}_1(N_{1D})(R_{11D}+jwL_{1(p)D}) + \dot{I}_2(N_{2D})jw(L_{2(1)D}-L_{2(p)D}) - \dot{I}_3(N_{3D})jw(L_{3(1)D}-L_{3(p)D})$$

Substituting (56), (57), (58) and (59) in (52), the following results.

$$(60)\quad \dot{E}_{LN1} = (N_{1A})\dot{I}_{pA}(R_{pA}+jwL_{p(1)A}) - \dot{I}_1(N_{1A})^2\left[R_{11A}+jwL_{1(p)A}\right] - N_{1A}\dot{E}_{pA} - \dot{I}_2(N_{1A})(N_{2A})jw(L_{2(1)A}-L_{2(p)A}) - \dot{I}_3(N_{1A})(N_{3A})jw(L_{3(1)A} - L_{3(p)A}) + N_{1B}\dot{I}_{pB}(R_{pB}+jwL_{p(1)B} - \dot{I}_1(N_{1B})^2\left[R_{11B}+jL_{1(p)B}\right] - N_{1B}\dot{E}_{pB} - \dot{I}_2(N_{1B})(N_{2B})jw(L_{2(1)B}- L_{2(p)B}) - \dot{I}_3(N_{1B})(N_{3B})jw(L_{3(1)B} - L_{3(p)B}) + N_{1C}\dot{I}_{pC}(R_{pC}+jwL_{p(1)C}) - \dot{I}_1(N_{1C})^2 (R_{11C}+jwL_{1(p)C}) - N_{1C}\dot{E}_{pC} + \dot{I}_2(N_{1C})(N_{2C})jw(L_{2(1)C}-L_{2(p)C}) - \dot{I}_3(N_{1C})(N_{3C})jw(L_{3(1)C} - L_{3(p)C}) - N_{1D}\dot{I}_{pD}(R_{pD}+jwL_{p(1)D}) - \dot{I}_1(N_{1D})^2(R_{11D}+jwL_{1(p)D}) + N_{1D}\dot{E}_{pD} - \dot{I}_2(N_{1D})(N_{2D})jw(L_{2(1)D}-L_{2(p)D}) + \dot{I}_3(N_{1D})(N_{3D})jw(L_{3(1)D} - L_{3(p)D})$$

Equation (60) can be rearranged to group the terms into five separate catagories:

$$(61)\quad \dot{E}_{LN1} = \left[-N_{1A}\dot{E}_{pA} - N_{1B}\dot{E}_{pB} - N_{1C}\dot{E}_{pC} + N_{1D}\dot{E}_{pD}\right]$$
$$+ (N_{1A})\dot{I}_{pA}(R_{pA}+jwL_{p(1)A}) + (N_{1B})\dot{I}_{pB}(R_{pB}+jwL_{p(1)B})$$
$$+ N_{1C}\dot{I}_{pC}(R_{pC}+jwL_{p(1)C}) - N_{1D}\dot{I}_{pD}(R_{pD}+jwL_{p(1)D})$$
$$- \dot{I}_1\left[(N_{1A})^2\left[R_{11A}+jwL_{1(p)A}\right] + (N_{1B})^2\left[R_{11B}+jwL_{1(p)B}\right]\right.$$
$$\left. + (N_{1C})^2\left[R_{11C}+jwL_{1(p)C}\right] + (N_{1D})^2\left[R_{11D}+jwL_{1(p)D}\right]\right]$$
$$- \dot{I}_2\left[(N_{1A})(N_{2A})jw(L_{2(1)A}-L_{2(p)A}) + (N_{1B})(N_{2B})jw(L_{2(1)B}-L_{2(p)B})\right.$$
$$\left. - (N_{1C})(N_{2C})jw(L_{2(1)C}-L_{2(p)C}) + (N_{1D})(N_{2D})jw(L_{2(1)D}-L_{2(p)D})\right]$$
$$- \dot{I}_3\left[(N_{1A})(N_{3A})jw(L_{3(1)A}-L_{3(p)A}) + (N_{1B})(N_{3B})jw(L_{3(1)B}-L_{3(p)B})\right.$$
$$\left. + (N_{1C})(N_{3C})jw(L_{3(1)C}-L_{3(p)C}) - (N_{1D})(N_{3D})jw(L_{3(1)D}-L_{3(p)D})\right]$$

Since

$$(62)\quad |\dot{E}_{pA}| = |\dot{E}_{pB}| = |\dot{E}_{pC}| = |\dot{E}_{pD}|$$

If

$$(63)\quad \dot{E}_{pA} = |E_{pA}|\angle 0°$$

$$(64)\quad \dot{E}_{pB} = |E_{pA}|\angle\frac{-180°}{NS};\ \dot{E}_{pC} = |E_{pA}|\angle\frac{-360°}{NS};\ \dot{E}_{pD} = |E_{pA}|\angle\frac{-540°}{NS}$$

The first group of Equation (61) can then be written:

$$(65)\quad \left[-N_{1A}\angle 0° - N_{1B}\angle\frac{-180°}{NS} - N_{1C}\angle\frac{-360°}{NS} + N_{1D}\angle\frac{-540°}{NS}\right]|\dot{E}_{pA}| =$$
$$(T.R.\angle\theta_R)|\dot{E}_{pA}|$$

which is the no load (neglecting excitation current) open circuit transformer line-to-neutral voltage of Phase 1.

The second group of terms can be expressed as follows, assuming balanced loads:

$$(66)\quad -\dot{I}_{pA}\sum_{S1}(\dot{N}_1)(R_p + jwL_{p(1)})$$

Where $\dot{N}_1$ signifies a phasor. The angles of these phasors and the signs are the same as in Equation (65).

The third group of terms can be expressed as follows:

$$(67) \quad -\dot{I}_1 \sum_{S1} (N_1)^2 (R_{11}+jwL_{1(p)})$$

where all terms of the summation are taken positive.

The fourth group of terms can be expressed as follows:

$$(68) \quad -j\dot{I}_2 \sum_{S21} (N_1)(N_2)\, w(L_{2(p)}-L_{2(1)})$$

where the sign of the term in the summation is determined as follows. If the assumed direction for the phase currents ($\dot{I}_1$ and $\dot{I}_2$) both enter the dot terminals or both leave the dot terminals of the particular secondary windings under consideration, the sign of the term is taken as positive.

The fifth group of terms can be similarly expressed as follows:

$$(69) \quad -j\dot{I}_3 \sum_{S31} (N_1)(N_3)\, w(L_{3(p)}-L_{3(1)})$$

where the sign of a term is determined as in Equation (68).

For balanced loads, the following relationships hold:

$$(70) \quad \dot{I}_2 = \dot{I}_1 \angle -120^\circ \; ; \; \dot{I}_3 = \dot{I}_1 \angle -240^\circ$$

If excitation current is neglected and if primary load current losses are transferred to the secondary, the following fundamental frequency volt-ampere relationship holds:

$$(71) \quad (NS)\left|E_{pA}\right|\left|I_{pA}\right| = 3\left|\dot{E}_{LN1}\text{ (open circuit)}\right|\left|\dot{I}_1\right|$$

or

$$(72) \quad \left|\dot{I}_{pA}\right| = \frac{3}{(NS)} \frac{\left|\overline{T.R.}\right|\left|\dot{E}_{pA}\right|\left|\dot{I}_1\right|}{\left|\dot{E}_{pA}\right|} = \frac{3\left|\overline{T.R.}\right|\left|\dot{I}_1\right|}{(NS)}$$

Since the total input power must equal total output power, and the total input reactive power must equal total output reactive power in Equation (71), the phasor angle between $\dot{E}_{LN1}$ (open circuit) and $\dot{I}_1$ must be the same as the phasor angle between $\dot{E}_{pA}$ and $\dot{I}_{pA}$.

Therefore,

$$(73)\quad \dot{I}_{pA} = \frac{3\left|\overline{T.R.}\right|}{NS}\ \dot{I}_1\ \angle -\theta_R$$

Substitution of Equation (65) thru (73) in Equation (61) results in the following expression.

$$(74)\quad \dot{E}_{LN1} = \dot{E}_{LN1}\ (\text{open circuit}) - \dot{I}_1\left[\frac{3\left|\overline{T.R.}\right|}{(NS)}\ \angle -\theta_R\ \sum_{S1}(\dot{N}_1)(R_p + jwL_{p(1)})\right.$$

$$+ \sum_{S1}(N_1)^2(R_{11}+jwL_{1(p)}) + \sum_{S21}(N_1)(N_2)\,w(L_{2(p)}-L_{2(1)})\ \angle -30^\circ$$

$$\left. + \sum_{S31}(N_1)(N_3)\,w(L_{3(p)}-L_{3(1)})\ \angle -150^\circ\right]$$

The expression inside the bracket in Equation (74) represents the internal impedance of the power transformer (under balanced load).

The impedance looking into the line-to-neutral terminals of Phase 1 is then given by the following expression:

$$(75)\quad Z_{eq} = \frac{3\left|\overline{T.R.}\right|}{(NS)}\left[\sum_{S1}(N_1)(R_p + jwL_{p(1)})\right]\ \angle -\theta_R + \sum_{S1}(N_1)^2(R_{11}+jwL_{1(p)})$$

$$+\left[\sum_{S21}(N_2)(N_1)(wL_{2(p)}-wL_{2(1)})\right]\angle -30^\circ$$

$$+\left[\sum_{S31}(N_3)(N_1)(wL_{3(p)}-wL_{3(1)})\right]\angle -150^\circ$$

where R_p is the total effective series resistance of the primary winding of a power stage plus any equivalent series resistance associated with internal impedance of the D.C. source. Likewise $L_{p(1)}$ includes the true leakage reactance plus any external equivalent series inductance. Z_{eq} will be in inverter P.U. ohms if resistances, inductive reactances and constants are in P.U. ohms

APPENDIX IV

Example of Internal Impedance Calculation and Its Use

Transformer Constants

The calculation of the leakage reactances of multiwinding transformers is a difficult problem. Certain simplifying assumptions in regard to leakage fluxes can be made. These assumptions reduce somewhat the complexity of the problem and are justified, to an extent, by the fact that the leakage reactances of transformers calculated in accordance with these assumptions check reasonably well with the measured values. The approximate method used here is that given in Reference 4.

The equivalent leakage reactance between two equal length windings, referred to the one with N_2 turns, is given by (all dimensions in inches):

$$(76) \quad X_e = \frac{20.1}{2} \; f \; \frac{N_2^2 M}{L} \; \left(d_3 + \frac{d_1}{3} + \frac{d_2}{3}\right) \times 10^{-8}$$

where d_1 and d_2 are the thickness of windings 1 and 2 respectively, d_3 is the spacing between the windings. M is mean length of turns in both windings. L is the length of winding.

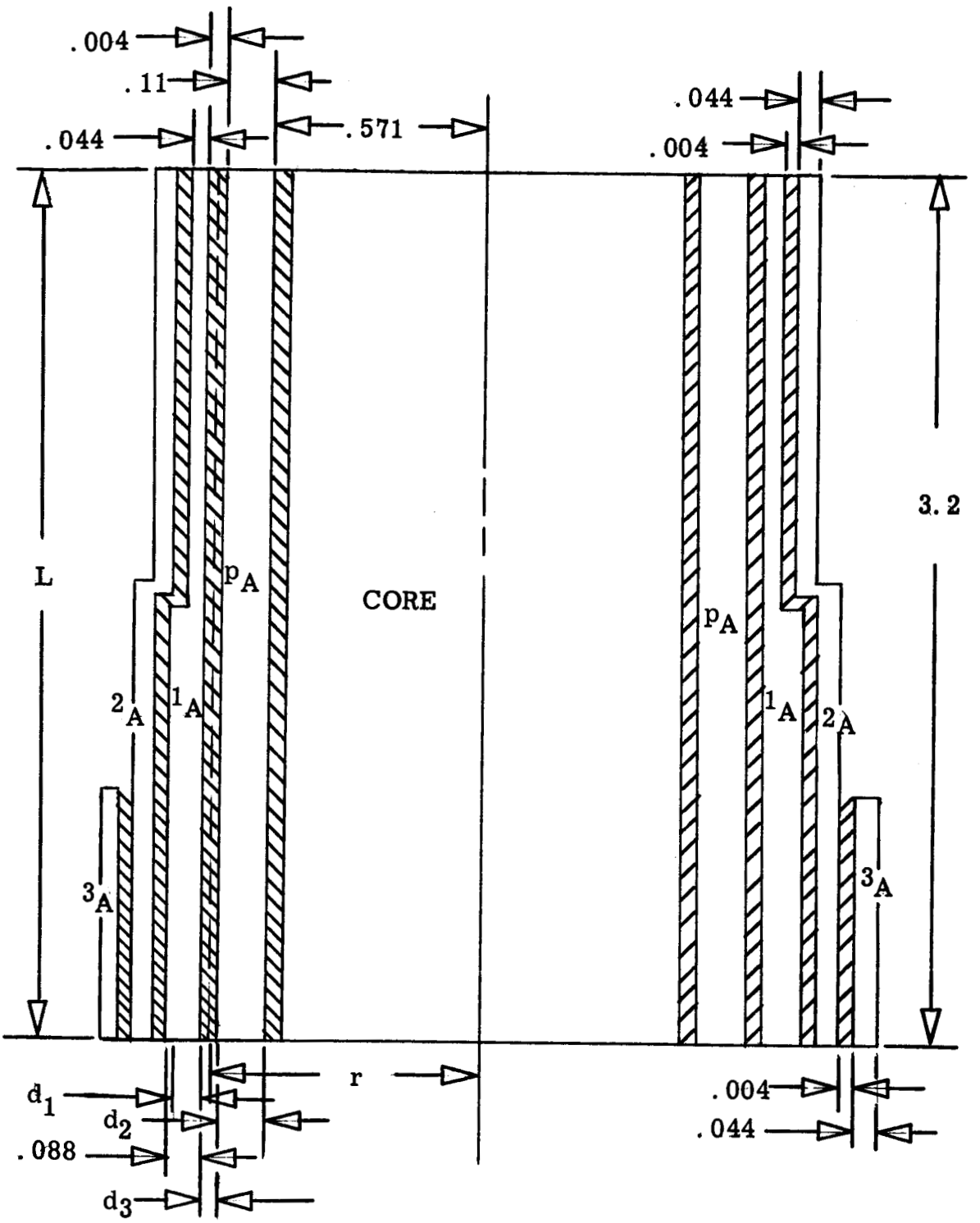
These dimensions along with other information on the winding positions and geometry are illustrated in Figure 24.

The various windings are not of equal length. This increases the difficulty of calculating the leakage reactance of such a design accurately by elementary formulas. Fortunately the problem at hand does not require that the leakage reactances be known to such a degree of accuracy to warrant the use of formidable "exact" methods.

The method used will be to adjust the thickness of each winding, while assuming them all to have the same length (L), so that the crossectional area of each winding remains the same.

For example for winding p_A and 1_A:

$$\begin{aligned} d_1 &= \frac{.088 + .044}{2} = .066 \\ d_2 &= .11 \\ d_3 &= .004 \\ L &= 3.2 \\ M &= 2\pi r = 2\pi\left(.571 + .11 + \frac{.004}{2}\right) = 4.29 \\ f &= 400 \text{ cps} \\ N_2 &= 50 \end{aligned}$$



NOTE: Not to scale; dimensions given are all in inches.

Figure 24. Sketch Used To Calculate Leakage Fluxes of Transformer A

Substitution of these values into the equation for X_e gives:

(77) $wL_{p(1)} \tilde{=} .00845$ ohms

The leakage reactances used in the Internal Impedance Calculations were calculated in a similar manner. The results are given in Table I (page 72).

Based on a 750 VA inverter: $V_B = 115$ volts
$I_B = 2.17$ amps
$Z_B = 53$ ohms

The transformer ratio ($\dot{\overline{T.R.}}$) can be calculated as follows:

(78) $$\dot{\overline{T.R.}} = \sum_{S1} \dot{N}_1 = -N_{1A} \angle 0° - N_{1B} \angle \frac{-180°}{4} - N_{1C} \angle \frac{-360°}{4} + N_{1D} \angle \frac{-540°}{4}$$

$$= -1.7 \angle 0° - 1.7 \angle -45° - .7 \angle -90° + .7 \angle -135°$$

(79) $$\dot{\overline{T.R.}} = -3.67 \angle -22.5 = 3.67 \angle 157.5$$

The sum defined in definition 13 will be calculated next. The effective internal resistance of the D.C. supply is approximately .0324 ohms. Therefore the R_p's used in the following equations will be taken as equal to .082 + .0324 ohms or .114 ohms.

(80) $$\sum_{S1} (\dot{N}_1)(R_p + jwL_{p(1)}) = \dot{N}_{1A}(R_{pA} + jwL_{p(1)A}) + \dot{N}_{1B}(R_{pB} + jwL_{p(1)B})$$
$$+ \dot{N}_{1C}(R_{pC} + jwL_{p(1)C}) + \dot{N}_{1D}(R_{pD} + jwL_{p(1)D})$$
$$= -1.7 \angle 0° (.144 + j.0085) - 1.7 \angle -45° (.114 + j.0085)$$
$$- .7 \angle -90° (.114 + j.022) + .7 \angle -135° (.114 + j.022) = -(.402 - j.126)$$

(81) $$\sum_{S1} (\dot{N}_1)(R_p + jwL_{p(1)}) = -.422 \angle -17.5° \text{ ohms or } -\frac{.422}{53} \angle -17.5 \text{ P.U. ohms}$$

Note that the first term of Equation (75) can now be evaluated using Equation (79) and Equation (81). Thus:

(82) First term Eq. (75) $= 3 \frac{|\dot{\overline{T.R.}}|}{(NS)} \sum_{S1} (\dot{N}_1)(R_p + jwL_{p(1)}) \angle -\theta_R$

$$= \frac{3}{4} (3.67)(-.422) \angle -17.5° - 157.5°$$

TABLE I

TRANSFORMER CONSTANTS

Transformer	R_p Ohms	$wL_{p(1)}$ Ohms	$wL_{1(p)}$ Ohms	$wL_{2(p)}$ Ohms	$wL_{2(1)}$ Ohms	$wL_{3(p)}$ Ohms	$wL_{3(1)}$ Ohms	N_1	N_2	N_3
A	.082	.0085	.0085	.018	.007	.017	.0065	1.7	1.46	.24
B	.082	.0085	.0085	.017	.006	.018	.0065	1.7	.24	1.46
C	.082	.022	.022	.018	.007	.0085	.007	.7	1.12	1.82
D	.082	.022	.022	.0845	.006	.018	.007	.7	1.82	1.12

(83) First term of Eq. (75) = $1.16 \angle 5°$ ohms or $\frac{1.16}{53} \angle 5°$ P.U. ohms.

Next consider the second term of Equation (75).

(84) Second term of Eq. (75) = $\sum_{S1} (N_1)^2 (R_{11} + jwL_{1(p)})$

$$= \sum_{S1} (N_1)^2 R_{11} + \sum_{S1} (N_1)^2 (jwL_{1(p)}).$$

The quantity $\sum_{S1} (N_1)^2 R_{11}$ is the total series resistance of the windings connected in Phase 1. Calculated from wire size and length it equals .85 ohm; therefore,

(85) Second term of Eq. (75) = $.85 + (N_{1A})^2 jwL_{1(p)A} + (N_{1B})^2 jwL_{1(p)B}$

$$+ (N_{1C})^2 jwL_{1(p)C} + (N_{1D})^2 jwL_{1(p)D}$$

$$= .85 + j(1.7)^2 (.0085) + j(1.7)^2 (.0085) + j(.7)^2 (.022) + j(.7)^2 (.022).$$

(86) Second term of Eq. (75) = $.85 + j.0706$ ohms or $\frac{.85 + j.0706}{53}$ P.U. ohms.

Next consider the third term of Equation (75).

(87) Third term of Eq. (75) = $\left[\sum_{S21} (N_2)(N_1)(wL_{2(p)} - wL_{2(1)}) \right] \angle -30°$

$$= \left[-(N_{1A})(N_{2A})(wL_{2(1)A} - wL_{2(p)A}) - (N_{1B})(N_{2B})(wL_{2(1)B} - wL_{2(p)B}) \right.$$

$$\left. + (N_{1C})(N_{2C})(wL_{2(1)C} - wL_{2(p)C}) - (N_{1D})(N_{2D})(wL_{2(1)D} - wL_{2(p)D}) \right] \angle -30°$$

$$= \left[-(1.7)(1.46)(.018 - .007) - (1.7)(.24)(.017 - .006) + .7(1.12)(.018 - .007) \right.$$

$$\left. - (.7)(1.82)(.0085 - .006) \right] \angle -30°$$

$$= -.0264 \angle -30° = -.0228 + j.0132.$$

(88) Third term of Eq. (75) = $.0228 + j.0132$ ohms or $\frac{.0228 + j.0132}{53}$ P.U. ohms.

Next consider the fourth term of Equation (75).

(89) Fourth term of Eq. (75) $= \left[\sum_{S31} (N_3)(N_1)(wL_{3(p)} - wL_{3(1)})\right] \angle -150°$

$= \Big[-(N_{1A})(N_{3A})(wL_{3(p)A} - wL_{3(1)A}) - (N_{1B})(N_{3B})(wL_{3(p)B} - wL_{3(1)B})$

$- (N_{1C})(N_{3C})(wL_{3(p)C} - wL_{3(p)C}) + (N_{1D})(N_{3D})(wL_{3(p)D} - wL_{3(1)D})\Big] \angle -150°$

$= \Big[-(1.7)(.24)(.017 - .0065) - (1.7)(1.46)(.018 - .0065)$

$-(.7)(1.82)(.0085 - .007) + (.7)(1.12)(.018 - .007)\Big] \angle -150°$

$= -.0261 \angle -150° = .0226 + j.0130.$

(90) Fourth term of Eq. (75) $= .0226 + j.0130$ ohms or $\frac{.0226 + j.0130}{53}$ P.U. ohms.

Substituting the values of Equations (83), (86), (88) and (90) into Equation (75):

(91) $\dot{Z}_{eq} = 1.16 + j.1 + .85 + j.0706 - .0228 + j.0132 + .0226 + j.0130.$

Collecting terms:

(92) $\dot{Z}_{eq} = 2.01 + j.1968$ ohms or $\frac{2.01 + j.1968}{53}$ P.U. ohms.

Referring back to Figure 8, $\dot{Z}_1$ can now be calculated:

(93) $\dot{Z}_{eq} + R_F + jwL_F = 2.01 + j.1968 + .32 + j(2.512)5 = 2.33 + j\,12.69$ ohms.

$C_{eq} = 3$ mfd ; $X_C = 132$ ohms.

(94) $\dot{Z}_p = \frac{(2.38 + j\,12.59)(-j\,132)}{2.38 - j\,119.41} = 2.61 + j\,13.9$ ohms.

(95) $\dot{Z}_p + \dot{Z}_{C.T.} = 2.61 + j\,13.9 + 0.383$ ohms.

(96) $\dot{Z}_1 = 3.00 + j\,13.9 = 14.3 \angle 77.8°$ ohms,

or

(97) $\dot{Z}_{1P.U.} = \frac{14.3}{53} \angle 77.8° = .27 \angle 77.8°$ P.U. ohms

If the phasor $\Delta\dot{I}$ has its angle with reference to a voltage, V_2, θ_2 degrees ahead of the phase voltage of the phase in which differential current loop is placed, it is desirable to have:

(98) $\theta_o - \theta_1 - \theta_2 \tilde{=} -90°$.

θ_o will generally vary between 0° and 15° depending on the load. For example:

at full load unity P. F., Equation (14) gives

$$\tan \theta_o = \frac{\sin (77.8°)}{\frac{1}{.27} + \cos 77.8°} = .249,$$

$$\theta_o = 14°.$$

at full load .7 P. F. lag

$$\tan \theta_o = \frac{\sin (77.8° - 45°)}{\frac{1}{.27} + \cos (77.8° - 45°)} = .119,$$

$$\theta_o = 6.8°.$$

at no load condition $\theta_o = 0°$.

As is customarily done with a-c generator parallel systems, the differential current sensing loop will be connected in phase C (refer to Figure 25), with $V_{LNC} = V\angle 0°$ then $V_{LLAC} = \sqrt{3}\ V\ \angle 30°$ is a phase voltage $\theta_2 = 30°$ ahead of the phase where differential current is sensed. At full load unity power factor, Equation (24d) becomes

(99) $$\Delta \dot{I} = \frac{\Delta E}{Z_1} \angle 14° - 77.8 - 30° = \frac{\Delta E}{Z_1} \angle -93.8°,$$

and if one of the inverters has an internal voltage greater than the average, it will result in that inverter taking more lagging reactive (in reference to V_{LLAC}) current than the average and its "reactive" load division circuit would need to reduce the "excitation" voltage (d-c voltage applied to power stages) of that inverter.

The gain needed in this "reactive" load division circuit may be calculated using the closed loop voltage regulation characteristics of a single unit as follows:

Define $E_{F.L.}$ to be the "internal" developed voltage (Thevenin's equivalent voltage) needed to maintain a full load terminal voltage, defined to be $V_{F.L.}$.

Then:

(100) $$E_{F.L.} = \frac{|\dot{Z}_1 + \dot{Z}_L|}{Z_L} V_{F.L.} = \frac{1}{K} V_{F.L.}.$$

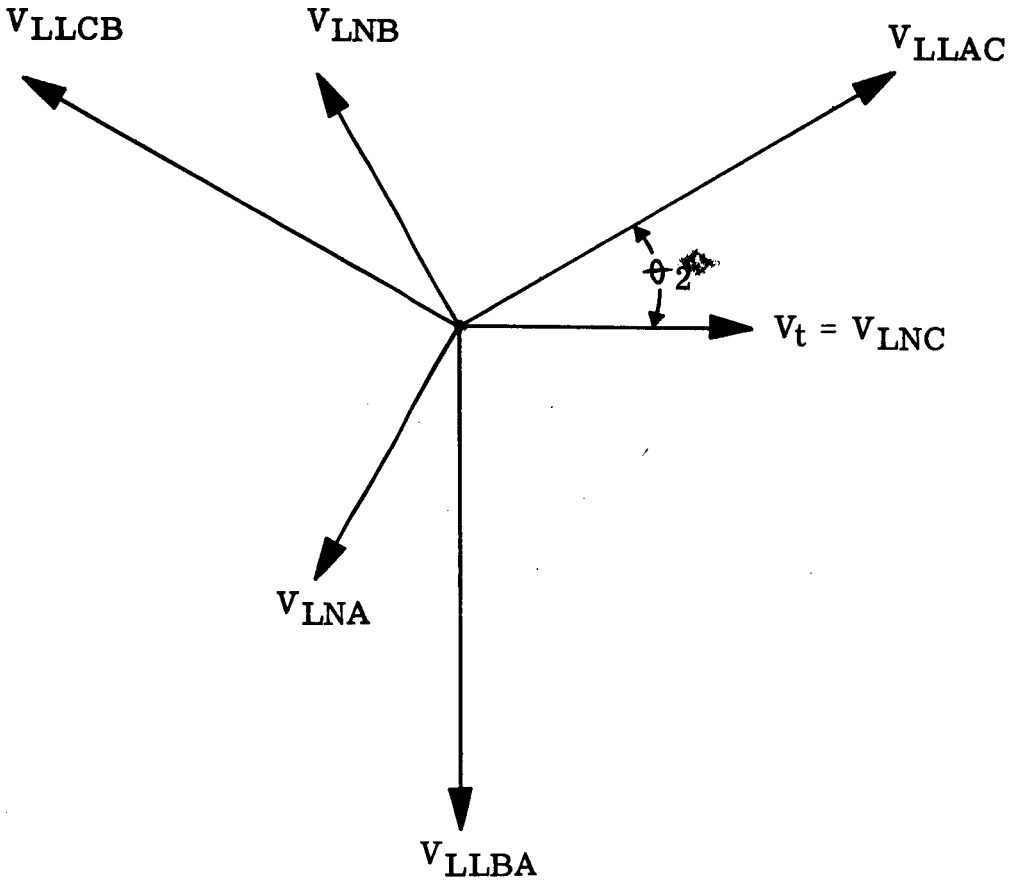


Figure 25. Phasor Diagram of Terminal Voltages
Line-To-Line - LL
Line-To-Neutral - LN

Define $V_{N.L.\ REG.}$ to be the terminal voltage under no load with the voltage regulator loop operating.

Define $V_{F.L.\ REG.}$ to be the terminal voltage under full load with the voltage regulator loop operating.

If closed loop voltage regulation is ± .7 volt = ± .0061 P.U. volts and assuming $V_{N.L.\ REG.} = 1.$ P.U. and $V_{F.L.\ REG} = .9939$ P.U. volts

$$(101)\quad \frac{\partial E}{\partial V_S} = -\left|\frac{E_{F.L.} - V_{N.L.\ REG.}}{V_{N.L.\ REG.} - V_{F.L.\ REG.}}\right| = -\left|\frac{\frac{|\dot{Z}_1+\dot{Z}_L|}{Z_L}\ (.9939) - 1.}{1-.9939}\right|$$

For Full Load .7 P.F. lag.

$$(102)\quad \frac{\partial E}{\partial V_S} = \left|\frac{|.27\angle 77.8° + 1\angle 45°|\ (.9939) - 1.}{.0061}\right|,$$

$$(103)\quad \frac{\partial E}{\partial V_S} = -38.$$

where V_S = voltage to sensing circuit = $V_{L.N.}$

Assuming a 115 ± .2 volt individual unit voltage setting,

$$(104)\quad V_{1L} = 1.00174 \text{ P.U. volts max.}$$

$$(105)\quad \text{and } V_o = V_{pL} = 1.\text{ P.U.}$$

Equation (33) becomes:

$$(106)\quad \Delta E = |E_{pL} - E_o| = (1 - 1.00174)\frac{\partial E}{\partial V_S} + \frac{1}{K}(1.00174 - 1) + \frac{\partial E}{\partial I_{DQ}}(\Delta I)$$

$$(107)\quad \Delta E = .0682 + \frac{\partial E}{\partial I_{DQ}}(\Delta I).$$

If the design objective is to assure that the load unbalance will never exceed 10%, the maximum allowable ΔE can be obtained from the expression:

$$(108)\quad \Delta I_{max} = .1 \text{ P.U.} = \frac{\Delta E_{max}}{Z_1} = \frac{\Delta E_{max}}{.27},$$

(109) $\Delta E_{max} = .027 = .0682 + \frac{\partial E}{\partial I_{DQ}} (.1)$, so

(110) $\frac{\partial E}{\partial I_{DQ}} = \frac{.027 - .0682}{.1} = -.412.$

This is the required gain of the "reactive" load division circuit expressed in P.U. volts droop per load current unbalance in P.U. Since the reference voltage is $V_{LLAC} = \sqrt{3}V/30°$ (see Figure 25), 60° lagging loads would appear as a 90° lagging current with respect to the reference voltage. Therefore, the "reactive" load division circuit should be made most sensitive to 60° lagging loads.

APPENDIX V

Block Diagram and Schematic Diagram of the Inverter/Converter Test Models to be Used to Demonstrate Parallel Operation

The circuits which are proposed to permit successful parallel operation of inverters or converters have been described in the text of this report and are shown schematically in Figures 9, 10, 12, and 14. Figure 26 is a block diagram which shows how these four circuits are interconnected with a complete static inverter. These four circuits are repeated schematically on Figure 27 with the complete schematic diagram of the Inverter/Converter test model. The block diagram is drawn as a schematic diagram overlay to help identify circuit functions.

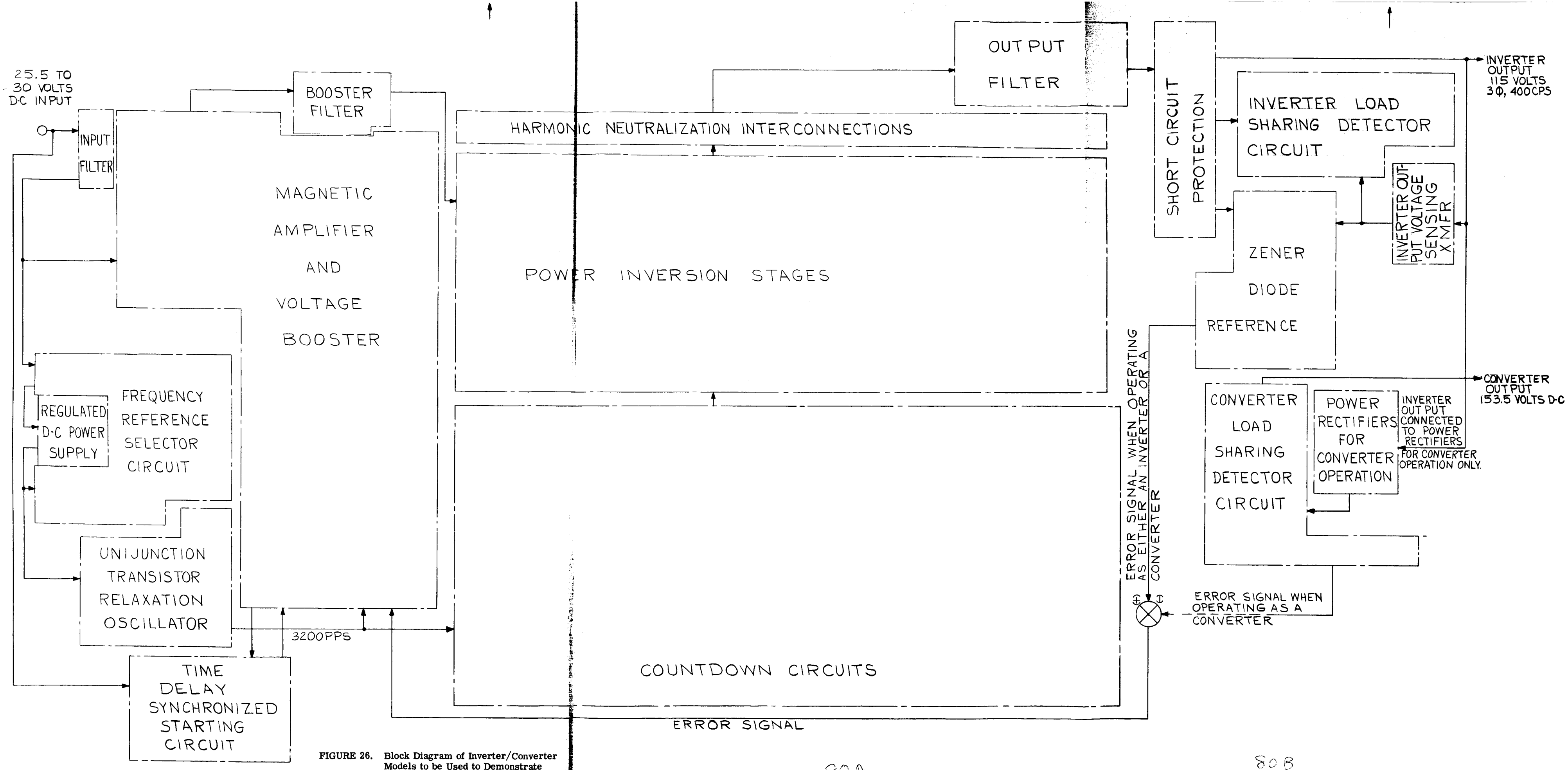


FIGURE 26. Block Diagram of Inverter/Converter Models to be Used to Demonstrate Parallel Operation

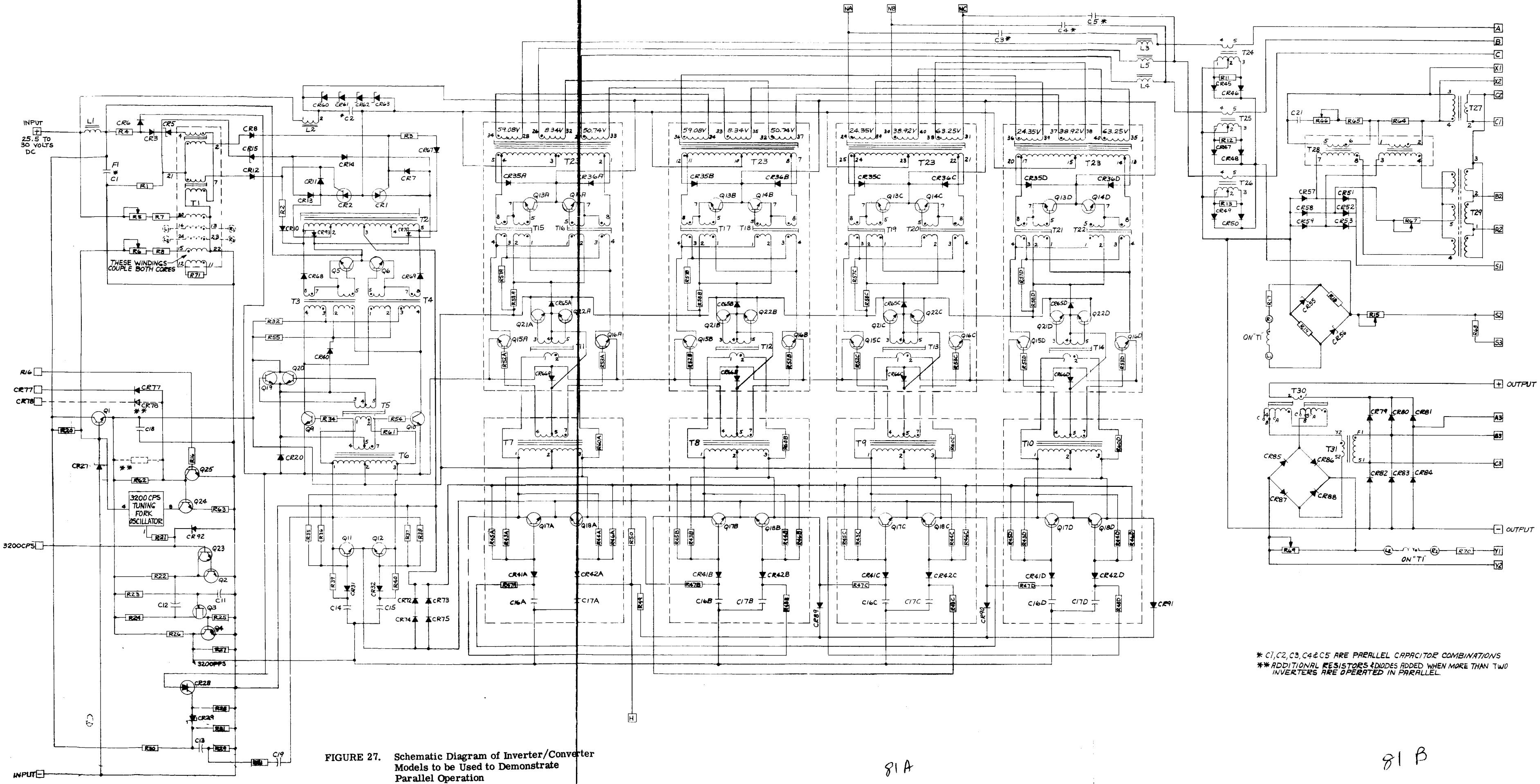


FIGURE 27. Schematic Diagram of Inverter/Converter Models to be Used to Demonstrate Parallel Operation

81A

81B

NOMENCLATURE

A = Square-wave voltage applied to primary of inverter output transformer, $A\angle 0°$.

B = $A\angle -45°$

C = $A\angle -90°$

C_{eq} = $C_{LN}+3C_{LL}$.

C_{IL} = Capacitance connected line-to-line between output phases. (Farads).

C_{LN} = Capacitance connected line-to-neutral in each output phase. (Farads).

C. T. = Current Transformer

D = $A\angle -135°$

d_1, d_2, d_3, L, M, and N_2 = These symbols are defined on pages 69 and 70.

E = Magnitude of internal voltage of a single static inverter operated "open loop" or unregulated.

E_{CA} = RMS value of fundamental voltage supported by core leg A.

E_{CB} = RMS value of fundamental voltage supported by core leg B.

E_{CC} = RMS value of fundamental voltage supported by core leg C.

E_{CD} = RMS value of fundamental voltage supported by core leg D.

$E_{F.L.}$ = Magnitude of the internal voltage with full load and $V_{F.L. Reg.}$ voltage at the output terminals.

e_k = Instantaneous value of E_k, k = 0, 1, 2.

E_{LN} = Magnitude (rms) of the line-to-neutral terminal voltage.

E_{LN1} = RMS value of the fundamental line-to-neutral output voltage from phase 1 of the output transformer.

E_{pA} = RMS value of fundamental primary voltage of power-stage-A.

E_{pB} = RMS value of fundamental primary voltage of power-stage-B.

E_{pC} = RMS value of fundamental primary voltage of power-stage-C.

E_{pD} = RMS value of fundamental primary voltage of power-stage-D.

E_{pL} = Magnitude of internal voltage of unit when operating in a loaded parallel system. (rms).

E_o = Magnitude of internal voltage if unit was adjusted to deliver a current equal to the average current. (rms).

E_1 = Magnitude of internal voltage of single static inverter unit. (rms).

E_{1A}, E_{2A}, E_{3A} = RMS value of fundamental secondary voltages of power-stage-A output transformer. (See Figure 20)

E_{1B}, E_{2B}, E_{3B} = RMS value of fundamental secondary voltages of power-stage-B output transformer. (See Figure 21)

E_{1C}, E_{2C}, E_{3C} = RMS value of fundamental secondary voltages of power-stage-C output transformer. (See Figure 22)

E_{1D}, E_{2D}, E_{3D} = RMS value of fundamental secondary voltages of power-stage-D output transformer. (See Figure 23)

E_{1L} = Magnitude of internal voltage of unit when operating as a loaded single unit system. (rms).

f = Frequency (cps).

I_{ac} = Magnitude (rms) of the line current of one output phase.

I_B = Value of the phase current rating of the inverter used in this study.

I_C = Magnitude (rms) of the current in output phase C.

I_{DQ} = $Q(\dot{I}_1-\dot{I}_o)$ = Magnitude of in-quadrature component of differential current. (rms).

I_{DR} = $R(\dot{I}_1-\dot{I}_o)$ = Magnitude of in-phase component of differential current (rms).

i_k = Instantaneous value of I_k, $k = 0, 1, 2$.

I_{LN1} = Transformer secondary line-to-neutral voltage of phase 1. (rms).

I_{Lp} = Magnitude of total load current in parallel system. (rms).

I_{pA} = RMS value of fundamental current in primary of power-stage-A.

I_{pB} = RMS value of fundamental current in primary of power-stage-B.

I_{pC} = RMS value of fundamental current in primary of power-stage-C.

I_{pD} = RMS value of fundamental current in primary of power-stage-D.

I_{Qo} = Magnitude of in-quadrature component of $\dot{I}_o$. (rms).

I_{Q1} = Magnitude of in-quadrature component of $\dot{I}_1$. (rms).

I_{Ro} = Magnitude of in-phase component of $\dot{I}_o$. (rms).

I_{R1} = Magnitude of in-phase component of $\dot{I}_1$. (rms)

I_{R64} = Magnitude (rms) of the current in R64.

I_o = Magnitude of average of total current from all units. (rms).

I_1 = Magnitude of line current of unit under consideration. (rms).

I_1, I_2, I_3 = Static-inverter output transformer secondary phase currents in per-unit (Appendix III).

$K = \left|\frac{Z_L}{\dot{Z}_1+\dot{Z}_L}\right|$.

$K_A = \frac{\partial E}{\partial I_{DQ}}$ = Rate of change of internal voltage magnitude with respect to in-quadrature components of differential current.

L_F = Inductance of output filter choke. (Henries).

L_{pp}, L_{11}, L_{22}, L_{p1}, L_{12}, L_{23}, $L_{p(1)}$, etc. = See Appendix III, pages 53, 55, 56, and 57, for definitions.

N = Number of units in parallel.

N_S = Number of power stages in each inverter.

N_{1A} = Phase 1 secondary winding turns (in P.U. based on one-half the primary winding turns) in stage A of the output transformer. The numerical subscript (1, 2, or 3) refers to the output phase in which the turns are connected. The letter subscript (A, B, C, or D) refers to the power stage in which the winding occurs.

Power Stage A = Inverter power stage with square-wave output voltage A $\angle 0°$

Power Stage B = Inverter power stage with square-wave output voltage A $\angle -45°$

Power Stage C = Inverter power stage with square-wave output voltage A $\angle -90°$

Power Stage D = Inverter power stage with square-wave output voltage A $\angle -135°$

$Q(I_1-I_o)$ = See I_{DQ}.

$Q_{\theta 2}(\dot{I}_1-\dot{I}_o)$ = The component of the differential current that is at right angles with a phasor that leads V_t by $\theta_2°$.

R_F = Resistance of output filter choke. (ohms).

$R(I_1-I_o)$ = See I_{DR}.

R_p = Resistance of 1/2 output transformer primary winding (ohms). Subscript A, B, C, or D refers to a particular power stage.

R_S = Setting of voltage regulating adjustment.

R_{SO} = Setting of voltage regulating adjustment so that when the unit is operating in the parallel system, $\dot{I}_1 = \dot{I}_o$.

R_{11} = Resistance of output-transformer secondary windings in output phase 1 (ohms). Additional subscript A, B, C, or D, refers to the resistance of secondary winding #1 in one particular power stage.

R_{22}, R_{33} = Same as R_{11} except R_{22} refers to output phase 2 and R_{33} refers to output phase 3.

$R_{\theta 2}(I_1-I_o)$ = The component of the differential current that is in phase with a phasor that leads V_t by $\theta_2°$.

t = time (seconds)

TFO = An acronym meaning Tuning Fork Oscillator.

T.R. = Transformer ratio. See Appendix III, page 57, for definition.

U_q' = Volume of the magnetic core of the quadratic transformer defined by Figures 5 and 6.

U_q = Volume of the magnetic core of a quadratic transformer.

U_s' = Volume of the magnetic core of a single-phase transformer using the maximum dimensions of Figures 5 and 6.

U_s = Volume of the magnetic core of a single-phase transformer.

UTRO = An acronym meaning Unijunction Transistor Relaxation Oscillator.

V_{AC} = Magnitude (rms) of the line A-to-line C terminal voltage.

V_B = Value of the line-to-neutral voltage ratings of inverter used in this study.

V_{BA} = Magnitude (rms) of the line B-to-line A terminal voltage.

V_{CB} = Magnitude (rms) of the line C-to-line B terminal voltage.

$V_{F.L.}$ = Magnitude (rms) of the rated terminal voltage.

$V_{F.L.\ REG.}$ = Magnitude of the full-load regulated output-terminal voltage.

V_{LLAC}, V_{LLBA}, V_{LLCB}, V_{LNA}, V_{LNB}, V_{LNC} = Inverter terminal voltages which are defined on page 76.

V_{LN} = Magnitude (rms) of line-to-neutral terminal voltage.

$V_{N.L.\ REG.}$ = Magnitude of the no-load regulated output-terminal voltage.

V_{pL} = Terminal voltage of unit when operating in a loaded parallel system. (rms).

V_S = The magnitude of a separate a-c voltage source which is applied to the voltage regulator sensing circuit of a static inverter.

V_t = Terminal or bus voltage. (rms).

V_o = Terminal or bus voltage if internal voltage is adjusted to deliver a current equal to the average current. (rms).

V_{1L} = Terminal voltage of unit when operating as a loaded single unit system. (rms).

V_2 = A voltage phasor that leads the terminal voltage by $\theta_2°$.

w = $2\pi f$

X_e = The equivalent reactance between two equal length windings, referred to the one with N_2 turns.

Z_B = Value of the minimum load impedance to be connected line-to-neutral on the inverter used in this study.

Z_{eq} = The internal per-phase impedance of the inverter with the output filter and current transformer removed. (See Figure 8).

Z_L = Magnitude of single load impedance.

Z_{Lp} = Magnitude of parallel system load impedance. (ohms).

Z_p = The equivalent internal per-phase impedance of the inverter with the current transformer shorted. (See Figure 8).

Z_1 = Magnitude of internal impedance of unit under consideration.

ΔE, $\Delta\theta$, etc. = Incremental values of variable designated.

ΔI_Q = Specified allowable differential quadrature current.

ΔR_S = Incremental change in regulator adjustment.

ΔV_S = Incremental change in voltage applied to sensing circuit.

θ_o = Angle of phasor E_o with respect to phasor V_t.

θ_1 = Angle of internal impedance $\dot{Z}_1$.

θ_{1L} = Angle of phasor E_{1L}.

θ_2 = Angle of phasor θ_2 degrees ahead of terminal voltage.

θ = The magnetic flux defined on pages 9 and 10.

θ_R = Phase angle of the transformer ratio, T.R. See Figure 19, page 59, for illustration.

Ψ = Power factor angle of bus load.

$\frac{\partial E}{\partial I_{DQ}}$ = See K_A.

$\frac{\partial E}{\partial I_{DR}}$ = The gain of the converter differential current sensing circuit.

$\frac{\partial E}{\partial R_S}$ = Rate of change of internal voltage amplitude (rms) with respect to regulator adjustment.

$\frac{\partial E}{\partial V_S}$ = Rate of change of internal voltage amplitude (rms) with respect to voltage (rms) applied to sensing circuit.

$\dot{}$ = This symbol over a quantity designates the phasor representation of that quantity.

$\simeq$ = Sumbol meaning "approximately equal to".

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